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Date 8/26/02 Serial # 09/986,277 Priority Application Date 5/29/01

Your Name M. Lewis Examiner # _____

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08-26-02 [illegible] IN

08-26-02 P03:22 OUT

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What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-13

Problem: See Page 3 lines 22-25

" 4 " 1-3 & 22-25

" 5 " 1-7

" 17 " 12-21

Solution: See structure illustrated in claims

Staff Use Only	Type of Search	Vendors
Searcher: SPECKARD	Structure (#)_____	STN ✓
Searcher Phone: 308-6559	Bibliographic ✓	Dialog ✓
Searcher Location: STIC-EIC2800, CP4-9C18	Litigation_____	Questel/Orbit_____
Date Searcher Picked Up: 9/4/02	Fulltext ✓	Lexis-Nexis_____
Date Completed: 9/4/02	Patent Family_____	WWW/Internet_____
Searcher Prep/Rev Time: 40	Other_____	Other_____
Online Time: 70		

09/04/2002 09/986,277

04sep02 13:10:43 User267149 Session D305.1

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(c) 2002 INIST/CNRS
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(c) 2002 DECHEMA
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200256
(c) 2002 Thomson Derwent
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File 344:Chinese Patents Abs Aug 1985-2002/Aug
(c) 2002 European Patent Office
File 347:JAPIO Oct 1976-2002/Apr(Updated 020805)
(c) 2002 JPO & JAPIO
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STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

09/04/2002 09/986,277

Alerts have been run. See HELP NEWS 347 for details.
File 371:French Patents 1961-2002/BOPI 200209
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*File 371: This file is not currently updating. The last update is 200209.

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

09/04/2002 09/986,277

Set	Items	Description
S1	596943	(SEMICONDUCT?????(N1)DEVICE? ?)
S2	2437286	SEMICONDUCT?????
S3	7269	CC=B2560 Semiconductor devices
S4	5026	MC=S01-G02B
S5	99552	IC=G01R-031
S6	2515170	S1:S5
S7	104010	(MULTIPLE OR MULTI)(3N)(LAYER???? OR COAT?????? OR FILM???-????)
S8	88439	TRENCH???????? OR DITCH???? OR FURROW????
S9	17953	PARTIAL????(3N)(REGION? ? OR AREA? ? OR ZONE? ?)
S10	4108307	ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT????
S11	283761	(CONDUCT??????)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULT-ILAYER??? OR SPACER???)
S12	12071	CC=(B2110 OR B2160 OR B8130)
S13	4753	MC=(S05-A02 OR S05-D01A1A OR U11-C05C4)
S14	7730	IC=(A61N-001/04 OR A61N-001/06 OR A61B-005/04)
S15	4733	MC=(V05-D07C5C OR V07-F01A1)
S16	108339	IC=(H01J-029/89 OR G02B-006)
S17	4247673	S10:S16
S18	441637	(INSULAT?????? OR DIELECTRIC???)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR SPACER???)
S19	12817	MC=(U11-C06A1B OR U11-C07C3 OR U11-C08A1 OR U11-C08A6)
S20	27879	CC=(A5150 OR A7700 OR B2800 OR B2810 OR B2830)
S21	474033	S18:S20
S22	68566	(CONTROL OR MAIN)(3N)(ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT????)
S23	1317348	DOPE???? OR DOPA???? OR DOPE???? OR DOPA?????? OR DOPING - OR IMPURIT???????
S24	1383714	S22:S23
S25	14553	TIGBT OR CSTBT OR CARRIER()STORED()TRENCH OR IGBT OR GATE(-)BIPOLAR()TRANSISTOR? ?
S26	18089	(GATE? ? OR OPENING? ?)(3N)(CAPACIT??????? OR CONDENS????)
S27	79204	BIP()TR OR BIPOLAR()TRANSISTOR? ?
S28	7869	S6 AND S25
S29	474	S28 AND S8
S30	201	S29 AND S17
S31	68	S30 AND S21
S32	17	S31 AND S22
S33	11	S32 AND S23
S34	11	RD (unique items)
S35	6	S32 NOT S33
S36	6	RD (unique items)
S37	51	S31 NOT S32
S38	3	S37 AND S26
S39	48	S37 NOT S38
S40	23	S39 AND S27
S41	23	RD (unique items)
S42	1	S41 AND S9
S43	22	S41 NOT S42
S44	12689	S6 AND S7
S45	123	S44 AND S8
S46	4	S45 AND S9

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

09/04/2002 09/986,277

S47	4	RD (unique items)
S48	119	S45 NOT S47
S49	62	S48 AND S17
S50	42	S49 AND S21
S51	1	S50 AND S22
S52	41	S50 NOT S51
S53	14	S52 AND S23
S54	1	S53 AND S25
S55	13	S53 NOT S54
S56	1	S55 AND S26
S57	12	S55 NOT S56
S58	2	S57 AND S27
S59	10	S57 NOT S58
S60	10	RD (unique items)

conductivity-type source **layer** through the first **conductivity**-type source **layer** to the second **conductivity**-type base **layer**.

An INDEPENDENT CLAIM is also included for a method of manufacturing a **semiconductor device** comprising forming in sequence first **trenches** for gates on a **semiconductor** substrate, gate **insulating films** within the first **trenches**, a gate **electrode** within the first **trenches** and on the gate **insulating films**, and interlayer **insulating films** on an entire surface of the substrate; removing a portion of the interlayer **insulating film**; and forming second **trenches** for contacts with the left portion of the interlayer **insulation film** and resist patterns used as mask.

USE - The device is useful for vertical metal oxide **semiconductor** field effect transistor and vertical insulated **gate bipolar transistor**.

ADVANTAGE - The device can be fabricated without mask alignment, thus scale down of the device is possible and the device property is improved.

DESCRIPTION OF DRAWING(S) - The figure shows an enlarged plan view of the top surface of the device.

First **conductivity**-type source **layer** (3)

Gate **insulating films** (4)

Portions of the first **conductivity**-type source **layer** (Wp)

pp; 21 DwgNo 2/12

34/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011528354
WPI Acc No: 1997-504835/199747
XRPX Acc No: N97-420464
Semiconductor component, e.g. **IGBT**, for high voltage inverter - has gate groove extending from p-type layer into n-type substrate and gate **insulating film** covering inner face of recess, n-type regions located on opposite sides of gate groove
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: NAKAMURA K; UENISHI A
Number of Countries: 004 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 19651108	A1	19971016	DE 1051108	A	19961209	199747	B
JP 9331063	A	19971222	JP 96332467	A	19961212	199810	
KR 97072199	A	19971107	KR 9662991	A	19961209	199846	
US 5894149	A	19990413	US 96762175	A	19961209	199922	
US 6111290	A	20000829	US 96762175	A	19961209	200043	
			US 98178767	A	19981026		
DE 19651108	C2	20001123	DE 1051108	A	19961209	200061	
KR 223198	B1	19991015	KR 9662991	A	19961209	200108	
US 6218217	B1	20010417	US 96762175	A	19961209	200123	
			US 98178767	A	19981026		
			US 2000618761	A	20000718		

Priority Applications (No Type Date): JP 9689439 A 19960411
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19651108	A1		45	H01L-029/739	
JP 9331063	A		25	H01L-029/78	
KR 97072199	A			H01L-021/328	
US 5894149	A			H01L-029/78	
US 6111290	A			H01L-029/745	Cont of application US 96762175 Cont of patent US 5894149
DE 19651108	C2			H01L-029/739	
KR 223198	B1			H01L-021/328	
US 6218217	B1			H01L-029/74	Cont of application US 96762175 Div ex application US 98178767 Cont of patent US 5894149 Div ex patent US 6111290

Abstract (Basic): DE 19651108 A
The component includes an n-type substrate (1), with a p-type layer (4) formed on the upper main surface of the substrate. A gate groove (70) in the substrate consists of a recess (7a), extending from the p-type layer into the substrate. A gate **insulating film** (7) covers an inner face of the recess, and a gate **electrode** (8) of a **conductor**, fills the recess.
Near one surface of the p-type layer is a pair of n-type regions

(5), located on opposite sides of the gate groove. Over the upper main surface is also formed a **main electrode layer** (10) with an **insulating film** (19) on the groove facing side coupled to the **doped** region and layer. On the lower substrate surface is formed a second p-type layer (3), whose surface carries a second **main electrode layer** (11). An **insulating layer** (15) is deposited between the gate grooves.

USE/ADVANTAGE - Also for e.g. thyristor with isolated gate to increase carrier carriers. High breakdown voltage without increasing gate capacity from OFF state of **IGBT**. **IGBT** is easily manufactured as ratio of distance between gate and emitter **trenches** w.r.t. width of gate **trench** is reduced so that both **trenches** can be formed in same arrangement.

Dwg.1/53

34/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014652438
WPI Acc No: 2002-473142/200251
Related WPI Acc No: 1993-054325; 1995-221795
XRPX Acc No: N02-373526
Insulated-gate power **semiconductor device** for industrial use inverter, has gate **electrodes** surrounding **insulating films** filled in **trenches**, such that films intervene between gate and **main electrodes** at opening of **trenches**
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: KITAGAWA M; OMURA I
Number of Countries: 004 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1209751	A2	20020529	EP 92307216	A	19920806	200251 B
			EP 20022322	A	19920806	

Priority Applications (No Type Date): JP 91354303 A 19911220; JP 91199343 A 19910808
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1209751	A2	E	66	H01L-029/739	Div ex application EP 92307216 Div ex patent EP 527600

Designated States (Regional): CH DE IT LI

Abstract (Basic): EP 1209751 A2
Abstract (Basic):
NOVELTY - A predetermined **main electrode** is arranged to close openings of the **trenches** (20), and to cover and contact a **semiconductor** layer (30). The gate **electrode** (24) are surrounded by **insulating films** (22) filled in the **trenches** such that the **insulating films** intervene between the gate and **main electrodes** at opening of **trenches**.
USE - Insulated gate-power **semiconductor device** for use in motor-controller for rail road vehicles, industrial use inverters, high voltage switching devices.
ADVANTAGE - Enhances the off-characteristics of **IGBT**, by preventing damage, by reducing on-resistance of the device, provides device with high **impurity** concentration region, and total injection efficiency.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of power **semiconductor device**.
Trench (20)
Insulating film (22)
Gate **electrode** (24)
Semiconductor layer (30)
pp; 66 DwgNo 2/102

34/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013589187
WPI Acc No: 2001-073394/200109
XRAM Acc No: C01-020854
XRPX Acc No: N01-055758
Trench-metal oxide **semiconductor** gate structure for e.g., vertical metal oxide **semiconductor** field effect transistor, has alternating **trenches** and source layers
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: NINOMIYA H
Number of Countries: 027 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1065710	A2	20010103	EP 2000305546	A	20000630	200109	B
JP 2001015743	A	20010119	JP 99186546	A	19990630	200120	
US 6359306	B1	20020319	US 2000606184	A	20000629	200224	

Priority Applications (No Type Date): JP 99186546 A 19990630
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1065710	A2	E	21	H01L-021/331	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
JP 2001015743	A		7	H01L-029/78	
US 6359306	B1			H01L-029/76	

Abstract (Basic): EP 1065710 A2
Abstract (Basic):
NOVELTY - A **trench**-metal oxide **semiconductor** (MOS) gate structure comprises first and second **conductivity**-type base **layers**, first and second **trenches**, first **conductivity**-type source **layer**, gate **insulating films**, gate **electrodes**, and first **main electrode**. The portions of the second **trenches** and that of the first **conductivity**-type source **layer** are alternately formed in the region among the first **trenches**.

DETAILED DESCRIPTION - A **trench**-MOS gate structure comprises second **conductivity**-type base **layer** on a first **conductivity**-type base **layer**, a first **conductivity**-type source **layer** (3) on the second **conductivity**-type base **layer**, first **trenches** formed in parallel to each other, gate **insulating films** (4) on wall surface of the first **trenches**, gate **electrodes** formed within the first **trenches** and on the second **conductivity**-type base **layer** via the gate **insulating film**, and a first **main electrode** within the second **trenches**. The portions of the second **trenches** and the portions of the first **conductivity**-type source **layer** (Wp) are alternately arranged in regions among the first **trenches**. The two **trenches** penetrate from the surface of the first

34/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011473150
WPI Acc No: 1997-451057/199742
Related WPI Acc No: 1996-414719
XRAM Acc No: C97-143968
XRPX Acc No: N97-375789
Insulated **gate bipolar transistors** with low on-state voltage - has five **semiconductor** layers formed in sequence, **trench** having opening formed in fifth **layer, insulating film, control electrode** and **main electrodes**
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: TAKAHASHI H
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 795911	A2	19970917	EP 96119114	A	19961128	199742	B
KR 97067933	A	19971013	KR 9656559	A	19961122	199843	
US 6040599	A	20000321	US 96721576	A	19960925	200021	
KR 218873	B1	19990901	KR 9656559	A	19961122	200104	
US 6221721	B1	20010424	US 2000484256	A	20000118	200125	

Priority Applications (No Type Date): JP 9654656 A 19960312
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 795911	A2	E	58	H01L-029/739	
Designated States (Regional): DE FR GB					
KR 97067933	A			H01L-029/76	
US 6040599	A			H01L-029/76	
KR 218873	B1			H01L-029/78	
US 6221721	B1			H01L-021/336	

Abstract (Basic): EP 795911 A
Insulated gate **semiconductor device** comprises in sequence, a first **semiconductor layer** of first **conductivity** type, second of second type, third of second type with higher **impurity** concentration than the second layer, fourth of the first type, fifth of second type, a **trench** extending from the surface of the fifth to at least through the fourth **layer** and with an **insulating layer** on its sidewalls, **control electrode** in the **trench** facing the fourth **layer** through the **insulating film**, first **main electrode** on the surface of the fourth and fifth layers, and a second **main electrode** on the second surface of the first **semiconductor** layer.
Also claimed is the method of making the device by deposition, implantation, and diffusion
USE - Insulated **gate bipolar transistors.**
ADVANTAGE - Current value capable of turn off is not decreased even if a structure for decreasing the on-state voltage is adopted.
Dwg.33/52

34/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010917768
WPI Acc No: 1996-414719/199642
Related WPI Acc No: 1997-451057
XRAM Acc No: C96-130714
XRPX Acc No: N96-349092

Insulated gate **semiconductor device** esp. U-type **IGBT** - has reduced ON voltage without decrease in turn-off current value

Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: TAKAHASHI H

Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 732749	A2	19960918	EP 96102102	A	19960213	199642	B
JP 8316479	A	19961129	JP 9654656	A	19960312	199707	
EP 732749	A3	19971008	EP 96102102	A	19960213	199813	
US 5751024	A	19980512	US 95566572	A	19951128	199826	
US 6001678	A	19991214	US 95566572	A	19951128	200005	
			US 97937163	A	19970925		
KR 199271	B1	19990701	KR 966882	A	19960314	200063	

Priority Applications (No Type Date): JP 9554564 A 19950314
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 732749	A2	E	38	H01L-029/739	
Designated States (Regional): DE FR GB					
JP 8316479	A		27	H01L-029/78	
EP 732749	A3			H01L-029/739	
US 5751024	A			H01L-029/74	
US 6001678	A			H01L-021/8234	Div ex application US 95566572
KR 199271	B1			H01L-029/72	

Abstract (Basic): EP 732749 A
An insulated gate **semiconductor device** comprises: (a) a **semiconductor** layer sequence of a first **conductivity** type first **layer**, a second **conductivity** type second **layer** with low **impurity** concn., a second **conductivity** type third **layer** with higher **impurity** concn. and a first **conductivity** type fourth **layer**; (b) a second **conductivity** type fifth **semiconductor layer** selectively provided in the surface of the fourth layer; (c) a **trench** which opens in the surface of the fifth layer and extends at least through the fourth **layer**; (d) an **insulating film** on the **trench** inner wall; (e) a **control electrode** in the **trench** and facing the fourth **layer** through the **insulating film**; (f) a first **main electrode** on the surface of the fourth and fifth layers; and (g) a second **main electrode** on the back surface of the first layer.
Also claimed is a method of mfg. an insulated gate

semiconductor device.
USE - Esp. as an **IGBT** with a **trench** MOS gate (U-type **IGBT**).
ADVANTAGE - The device has a decreased ON voltage, without decrease of the current value capable of being turned off and has low power consumption, small size, large capacity and high reliability.
Dwg.3/31

34/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009572225
WPI Acc No: 1993-265771/199334
XRAM Acc No: C93-118440
XRPX Acc No: N93-203839
Semiconductor device with vertical channel MOS gate structure - has reduced size and ON-resistance allowing high integration
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: HARADA M
Number of Countries: 004 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4242558	A1	19930819	DE 4242558	A	19921216	199334	B
GB 2264388	A	19930825	GB 9224693	A	19921125	199334	
JP 5226661	A	19930903	JP 9229561	A	19920217	199340	
US 5298780	A	19940329	US 92980691	A	19921124	199412	
GB 2264388	B	19950802	GB 9224693	A	19921125	199534	
DE 4242558	C2	19950921	DE 4242558	A	19921216	199542	

Priority Applications (No Type Date): JP 9229561 A 19920217
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4242558	A1		20	H01L-029/784	
JP 5226661	A		8	H01L-029/784	
US 5298780	A		19	H01L-029/06	
DE 4242558	C2		20	H01L-029/772	
GB 2264388	A			H01L-029/784	
GB 2264388	B			H01L-029/70	

Abstract (Basic): DE 4242558 A

A **semiconductor device** has (i) a second **conductivity** type second **semiconductor layer** between a first **semiconductor** layer and a selectively formed third **semiconductor layer**, both of first **conductivity** type; (ii) a recess extending from the top surface of the third layer through the second layer into the first **layer**; (iii) a **dielectric layer** on at least the recess inner wall in opposite relation to the second layer; (iv) a **control electrode** formed over the **dielectric layer** on the recess inner wall; (v) an **insulation layer** contg. a first **conductivity** type **impurity** and formed on part of the recess inner wall in opposite relation to the third layer; and (vi) a third layer section adjacent the recess, having uniform **impurity** concn. in the vertical direction along the recess.

Prodn. of a **semiconductor device** involves (a) forming a second **conductivity** type second **semiconductor layer** on a first main surface of a first **conductivity** type first **semiconductor layer**; (b) forming a recess which extends from the upper surface of the second layer into the first layer and

34/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009890068
WPI Acc No: 1994-169984/199421
XRPX Acc No: N94-133873
Voltage surge protection structure for smart power switch - has surface with p-type **trench** receiving diffusion which defines source while lateral canal delimiting diffusion is covered by gate on **insulating layer**
Patent Assignee: STMICROELECTRONICS SA (SGSA); SGS THOMSON MICROELTRN SA (SGSA)
Inventor: BARRET J; QUESSADA D
Number of Countries: 006 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 599745	A1	19940601	EP 93420458	A	19931119	199421	B
FR 2698486	A1	19940527	FR 9214478	A	19921124	199424	
JP 6224436	A	19940812	JP 93290300	A	19931119	199437	
US 5543645	A	19960806	US 93157362	A	19931123	199637	
US 5563436	A	19961008	US 93157362	A	19931123	199646	
			US 95479511	A	19950607		
US 5780895	A	19980714	US 93157362	A	19931123	199835	
			US 95573300	A	19951215		
EP 599745	B1	20010718	EP 93420458	A	19931119	200142	
DE 69330455	E	20010823	DE 630455	A	19931119	200156	
			EP 93420458	A	19931119		

Priority Applications (No Type Date): FR 9214478 A 19921124
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 599745	A1	F	9	H01L-027/02	
Designated States (Regional): DE FR GB IT					
FR 2698486	A1			H01L-023/62	
JP 6224436	A		7	H01L-029/784	
US 5543645	A		10	H01L-029/76	
US 5563436	A		9	H01L-029/76	Div ex application US 93157362
US 5780895	A			H01L-029/76	Cont of application US 93157362; Cont of patent US 5543645
EP 599745	B1	F		H01L-027/02	
Designated States (Regional): DE FR GB IT					
DE 69330455	E			H01L-027/02	Based on patent EP 599745

Abstract (Basic): EP 599745 A
A MOS transistor with vertical structure includes a number of cells which are obtained on a **semiconductor** substrate (O). The rear surface of the substrate is covered with a metallic layer (12) while p-type **trenches** (1) are defined on the cell surface. Each **trench** receives a ring shaped diffusion (2) that defines the source.
A lateral canal (4) limits the diffusion area being covered by an **insulating layer** (7) and a gate (6). The voltage surge

protection structure consists of an additional cell which has a structure identical with that of the transistor cells. The lateral dimensions of the protection cell are reduced.

USE/ADVANTAGE - For power MOS transistor with vertical structure and bipolar transistor with isolated gate. Can be obtained on transistor substrate without changing its design. Threshold voltage is well defined. Does not require alteration of transistor fabrication method.

Dwg.3/5

Abstract (Equivalent): US 5563436 A

A method for preventing a power transistor from reaching an avalanche breakdown condition, comprising:

providing a power transistor including a plurality of identical cells formed in a **semiconductor** substrate, each identical cell including a low **doped** well region of a second conductivity type disposed in the **semiconductor** substrate of a first conductivity type, the low **doped** well region having a deeper and more highly **doped** central region, source diffusion regions of the first conductivity type substantially peripheral to and within the low **doped** well region, a drain terminal disposed on a lower surface of the **semiconductor** substrate, a gate terminal disposed above an **insulating layer** disposed above the source diffusion regions, and a source terminal disposed above an upper surface of the central region of the low **doped** well region;

providing at least one substantially identical cell to the plurality of identical cells, electrically connected between the drain terminals and the gate terminals of the plurality of identical cells, the at least one additional cell having a smaller lateral sized low **doped** well region than the low **doped** well region of the plurality of identical cells;

applying a voltage across the drain and source terminals of the identical cells when the identical cells are in a non-**conducting** state; and

biasing the identical cells to a **conducting** state just before the voltage across the drain and source terminals causes an avalanche breakdown condition.

Dwg.3/5

US 5543645 A

A VDMOS or **IGBT**-type power transistor, comprising:

a plurality of identical active cells formed in an upper surface of a **semiconductor** substrate **doped** with a first conductivity type, each active cell including:

a low **doped** well region of a second conductivity type and having a deeper and more highly **doped** central portion;

source diffusion regions substantially peripheral to and within the low **doped** well region and having a highly **doped** level of the first conductivity type, the source diffusion regions thereby forming peripheral regions within the low **doped** well region;

a second **electrode** contacting an upper surface of the central portion of the low **doped** well region and the source diffusion regions;

a **control electrode** disposed on top of an **insulating layer** which is disposed over the peripheral regions; end

a first **main electrode** formed on a lower surface of the substrate; and

at least one additional cell manufactured according to the same steps as the active cells and disposed in parallel between the first **main electrode** and the **control electrode**, the at least one additional cell having a smaller lateral sized low **doped** well region than the identical cells such that the at least one additional cell has an avalanche threshold lower than an avalanche threshold of the plurality of identical active cells.

Dwg.3/6

34/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009857456
WPI Acc No: 1994-137312/199417
XRAM Acc No: C94-063465
XRPX Acc No: N94-107870
Insulated gate **semiconductor device** and - includes a buffer layer with highly **doped** regions and less highly **doped** regions to control collector current flow and provide a low ON-resistance
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: TAKAHASHI H
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 594049	A1	19940427	EP 93116565	A	19931013	199417	B
JP 6204481	A	19940722	JP 93234992	A	19930921	199435	
US 5569941	A	19961029	US 93135471	A	19931013	199649	
			US 95441787	A	19950516		
EP 594049	B1	20020130	EP 93116565	A	19931013	200209	
DE 69331512	E	20020314	DE 631512	A	19931013	200226	
			EP 93116565	A	19931013		

Priority Applications (No Type Date): JP 93234992 A 19930921; JP 92281664 A 19921020
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 594049	A1	E	40	H01L-029/10	
Designated States (Regional): DE FR GB					
JP 6204481	A		19	H01L-029/784	
US 5569941	A		33	H01L-029/74	Cont of application US 93135471
EP 594049	B1	E		H01L-029/10	
Designated States (Regional): DE FR GB					
DE 69331512	E			H01L-029/10	Based on patent EP 594049

Abstract (Basic): EP 594049 A
Device comprises: First region (1) of first type; second region (3,21) of second type formed on the first region, third region (4, 4a, 4b) of first type formed selectively in the second region; fourth region (5, 5a, 5b) of second type formed in the third region; fifth region (22) of second type formed in the bottom of the second region spaced from the third and fourth regions and having a higher **impurity** concn. than the second region; overlying insulation (7); **electrodes** (9, 10) connected to the first and fourth region; and a **control electrode**(s) formed on the **insulating layer**.
Methods for mfg. the device are claimed.
USE/ADVANTAGE - Esp. as an insulated **gate bipolar transistor**. Device achieves a low ON-resistance while also having improved durability against destruction since flow of collector current is suppressed for large current flows.
Dwg.1/22
Abstract (Equivalent): US 5569941 A

An insulated gate **semiconductor device**, comprising: a first **semiconductor** region of a first conductivity type; a second **semiconductor** region of a second conductivity type formed on the first **semiconductor** region; a third **semiconductor** region of the first conductivity type selectively formed in a top portion of the second **semiconductor** region; a fourth **semiconductor** region of the second conductivity type selectively formed in a top portion of the third **semiconductor** region; a fifth **semiconductor** region of the second conductivity type selectively formed in a bottom portion of the second **semiconductor** region being formed in the shape of flat stripes and having a higher concentration of **impurities** of the second type than the second **semiconductor** region; an **insulating layer** formed on the third and the fourth **semiconductor** regions; a first **main electrode** electrically connected to the first **semiconductor** region; a second **main electrode** electrically connected to the fourth **semiconductor** region; and a **control electrode** formed on the **insulating layer**; wherein the third **semiconductor** region comprises first and second portions laterally separated from each other, a **trench** is formed in a top portion of the second **semiconductor** region located between the first and second portions of the third **semiconductor** region, the **insulating layer** is formed on an inside wall of the **trench**, and the **control electrode layer** substantially covers the **insulating layer** in the **trench**.

(Dwg.1/22

34/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009770498
WPI Acc No: 1994-050349/199407
XRPX Acc No: N94-039674
Semiconductor insulated gate field effect device mfg. method - introducing opposite conductivity **impurities** into **semiconductor** through masking layer with two openings, using second masking layer to cover one opening and etching **semiconductor** through second window to define recess
Patent Assignee: PHILIPS ELECTRONICS NV (PHIG); PHILIPS ELECTRONICS UK LTD (PHIG); PHILIPS GLOEILAMPENFAB NV (PHIG); US PHILIPS CORP (PHIG)
Inventor: GOODYEAR A L; HUTCHINGS K M; WARWICK A M
Number of Countries: 002 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 583022	A2	19940216	EP 93202127	A	19930720	199407	B
JP 6209013	A	19940726	JP 93180162	A	19930721	199434	
US 5387528	A	19950207	US 9395972	A	19930722	199512	
EP 583022	A3	19960814	EP 93202127	A	19930720	199641	

Priority Applications (No Type Date): GB 9215653 A 19920723
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 583022	A2	E	16	H01L-021/336	
JP 6209013	A		10	H01L-021/336	
US 5387528	A		13	H01L-021/265	
EP 583022	A3			H01L-021/336	

Abstract (Basic): EP 583022 A
The insulated gate field effect device mfg. method involves defining a masking layer (6) with at least two spaced windows (6a,b) on a **semiconductor** body surface and introducing through the masking layer **impurities** to form regions of opposite conductivity to the **semiconductor** body region (4) adjacent the surface. A second masking layer (8), selectively removable w.r.t. the first mask layer, is patterned to leave a mask area (8a) covering one of the bottom mask layer windows (6a).

The **semiconductor** is etched through the second lower mask window (6b) to define a recess extending into the **semiconductor** body, with the introduced **impurities** forming a relatively highly **doped** opposite conductivity region beneath the masked area. The masks are removed. A gate **insulating layer** is defined on the recess surface or walls (9a) with a gate **conductive** region on the **insulating layer**. An opposite **conductivity** relatively low **doped** third region is formed, extending between the highly **doped** region and the recess and forming a **conduction** channel area adjacent the insulated gate structure. A fourth region forms a potential barrier with the low **doped** region to **control** the channel **conductive** path between the first

and fourth regions.

USE/ADVANTAGE - E.g. power **semiconductor device** with cells; power MOSFET, vertical or lateral IGFET; **IGBT**; suitable for integration with e.g. logic circuitry. Recess self-aligned to highly **doped** region.

Dwg.4/13

Abstract (Equivalent): US 5387528 A

The method of manufacturing a **semiconductor device** e.g. an insulated gate field effect (IGFET), involves providing a **semiconductor** body having a first region of one conductivity type adjacent one major surface, and forming a first masking layer on it, with at least two spaced apart mask windows. **Impurities** are introduced through the first masking layer for forming regions of opposite conductivity to the first region. A second masking layer is deposited, is selectively removable w.r.t. the first masking layer, and is patterned to leave a mask area covering the first mask window. The **semiconductor** body is etched through the second mask window to form a recess extending into the first region, while leaving the introduced **impurities** beneath the first mask window to form a relatively highly **doped** second region.

The two masking layers are removed to provide an insulated gate structure by forming a gate **insulating layer** in the recess and providing a gate **conductive** region on the **insulating layer**. A relatively lowly **doped** third region of the opposite conductivity is provided and extends between the relatively highly **doped** second region and the insulated gate structure to provide a **conduction** channel adjacent the insulated gate structure. A fourth region forms a potential barrier with the third region so that the channel area is controllable by the insulated gate structure between the fourth and first regions.

USE/ADVANTAGE - E.g. for **trench** type device having relatively flat surface enabling good coverage by subsequent layers. Avoids use of mask for defining third region.

3,4,8,12/1

3

which has a first region, near the upper surface of the second layer, and a further second region; (c) forming a **dielectric layer** and then a **control electrode** on the recess inner wall in the second region; (d) forming an **insulation layer**, contg. a first **conductivity** type diffusion source **impurity**, at least one the recess inner wall in the first region; and (e) diffusing the **impurity** from the **insulation layer** for selective formation of a first **conductivity** type third **semiconductor layer** in the second layer in contact with the recess, the third layer being longer than the first region in the thickness direction of the second layer.

USE/ADVANTAGE - The device is esp. a power MOSFET with a vertical channel MOS gate structure or an **IGBT**. It has reduced size and ON-resistance, thus allowing high integration.

e seco

Dwg.1/19

Abstract (Equivalent): DE 4242558 C

The **semiconductor device** described has a first **semiconductor** layer (1) of a first **conducting** type with a first and a second main surface, a second **semiconductor** layer (2) of a second **conducting** type formed on the first main surface, a third **semiconductor** layer (3) of the first **conducting** type formed selectively on the second layer, and a **trench** (40) stretching from the upper surface of the source region (5) through the third layer into the second layer. There is also a **dielectric layer** on at least one inner wall of the **trench**, a **control electrode** formed on the **dielectric layer**, and an **insulating layer** on a part of the inner wall of the **trench**.

USE/ADVANTAGE - Suitable for the **semiconductor** industries, in particular MOSFET design. Has a high integration density and is of low size comparatively, with a low input resistance.

Dwg.1/19

Abstract (Equivalent): GB 2264388 B

A **semiconductor device** comprising: a first **semiconductor layer** of a first **conductivity** type having first and second major surfaces; a second **semiconductor layer** of a second **conductivity** type formed on said first major surface; a third **semiconductor layer** of the first **conductivity** type selectively formed on said second **semiconductor** layer; a groove extending from a top surface of said third **semiconductor** layer through said second **semiconductor** layer into said first **semiconductor layer**; a **dielectric layer** formed at least on an inner wall of said groove which is in face-to-face relation to said second **semiconductor** layer; a **control electrode** formed on said inner wall of said groove covering said **dielectric layer**; and an **insulating layer** formed on a part of an inner wall of said groove which is in face-to-face relation to said third **semiconductor** layer and containing an **impurity** of the first conductivity type, a portion of said third **semiconductor** layer adjacent to said groove having a uniform **impurity** concentration in the vertical direction along said groove.

Dwg.1/1

09/04/2002 09/986,277

Abstract (Equivalent): US 5298780 A

Semiconductor device comprises an N channel MOSFET with a drain region (1) of N+type **semiconductor**, an N diffusion layer (2) of N type **semiconductor** and a body (3) of P type **semiconductor**, through which grooves (40) are formed from source regions (5). Grooves are filled with buried oxide films (15) including N type **impurities**. Source-**electrode** metal (6) covers source regions and body to short circuit them and is insulated from the buried gate **electrodes** by the buried oxide films. **Impurity** regions (5a) of relatively high concentration are formed adjacent to the grooves.

ADVANTAGE - Reduced ON resistance in reduced size, high integration device.

Dwg.1/19

34/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007922997
WPI Acc No: 1989-188109/198926
XRAM Acc No: C89-083214
XRPX Acc No: N92-037694
Insulated **gate bipolar transistor** - has **trench** within first region with **conductive layer** connected to first region and **electrode** to reduce vertical resistance
Patent Assignee: MITSUBISHI DENKI KK (MITQ)
Inventor: HARADA M
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 1125979	A	19890518	JP 87285807	A	19871111	198926	B
US 5079602	A	19920107	US 88195652	A	19880517	199205	
US 5173435	A	19921222	US 88195652	A	19880517	199302	
			US 91775442	A	19911015		

Priority Applications (No Type Date): JP 87285807 A 19871111
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 1125979	A		9		
US 5173435	A		9	H01L-021/265	Div ex application US 88195652 Div ex patent US 5079602

Abstract (Basic): US 5079602 A

The insulated **gate bipolar transistor** has a P-type well region (3) partially formed in a surface of an N negative-type epitaxial layer (2) formed on a p positive-type semi-**conductor** substrate (1). A **trench** (14) is formed in a central portion of the P-type well region (3), and an N positive-type emitter region (4) is formed in a surface of the P-type well region (3) around the **trench** (14). The N positive-type emitter region is provided thereon with an emitter **electrode** (7), extended into the **trench** (14) as a **conductive layer** to electrically connect a deep portion of the P-type well region (3) with N positive-type emitter region (4). Thus, vertical, resistance of the P-type well region (3) is reduced, whereby base-to-emitter resistance of an NPN transistor defined by the N negative-type epitaxial layer (2). The P-type well region (3) and the N positive-type emitter region (4) is reduced to prevent a latch-up of a parasitic PNPN thyristor. Furthermore, by means of **impuritity** diffusion on the side wall and/or the bottom of the **trench** (14), the high **impurity** concentration region is formed in the deep portion of the P-type well region (3). Especially, lateral **impurity** diffusion results in reducing the resistivity of the region of the P-type well just under the N positive-type emitter region (4). This prevents the NPN transistor from being in **conductive** state. Thus, the latch-up of the parasitic PNPN thyristor is further prevented.

ADVANTAGE - Can effectively prevent latch-up phenomenon. Has

structure suitable for high current capacity and implementation of cell arrangement with high density. (First major country equivalent to J01125979) (9pp Dwg.No.8/8) (Previously notified in week 9205/Printed in week 920

Dwg.8/8

Abstract (Equivalent): US 5173435 A

The method involves the step of preparing a conductivity type **semiconductor** substrate having two major surfaces forming a second **conductivity** type **semiconductor layer** opposite to the first conductivity type is formed on the first major surface of the **semiconductor** substrate. A region of the first conductivity type is formed in a surface of the **semiconductor** layer. A second region of the second conductivity type is formed in a surface of the first region. An **insulation film** is formed on the surface of the first region and extends between the surfaces of the **semiconductor** layer and second region. A **control electrode** is formed on the **insulation film**. A **trench** is formed in first region through the second region. The **trench** is filled with a **conductive** material including the step of **doping** the **conductive** material with an **impurity**. The **impurity** is diffused in the first region around the **trench** by employing the **conductive** material as a diffusion source to form a high concentration **impurity** diffusion region of the first conductivity type. A **electrode** is formed on the second region and the **conductive** material to electrically connect the second region and the **conductive** material forming a second **electrode** is formed on the second major surface of the **semiconductor** substrate.

ADVANTAGE - Insulated **gate bipolar transistor** prevents latch-up phenomenon. Suitable for high current capacity and high density cell arrangement. (Dwg.5/8)

34/3,AB/11 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05716263
HIGH BREAKDOWN STRENGTH **SEMICONDUCTOR DEVICE** AND ITS MANUFACTURING METHOD

PUB. NO.: 09-331063 [JP 9331063 A]
PUBLISHED: December 22, 1997 (19971222)
INVENTOR(s): UENISHI AKIO
NAKAMURA KATSUMITSU
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-332467 [JP 96332467]
FILED: December 12, 1996 (19961212)

ABSTRACT

PROBLEM TO BE SOLVED: To enable the high breakdown strength to be gained without increasing the gate capacity in the off state of a gate **trench** type high breakdown strength **IGBT** by providing an **insulating layer** on the position held by gate **trenches** in a **semiconductor** substrate.

SOLUTION: The second conductivity type the first **impurity** layer 4 is formed on the first main surface of the first conductivity type **semiconductor** substrate 1 while a gate **insulating film** 7 and a gate **electrode** 8 are formed in a **trench** part 7a formed from the first **impurity** layer 4 extending over the **semiconductor** substrate 1 so as to provide gate **trenches** 70. Besides, pairs of the first conductivity type **impurity** regions 5 holding the gate **trenches** 70 are formed to cover the first main surface further providing the first **main electrode** layer 10 over the gate **trenches** 70 through the intermediary of **insulating films** 18-20. Next, the second **conductivity** type second **impurity layer** 3 is formed on the second main surface of the substrate 1 further to form the second **main electrode** layer 11 on the surface of this layer 3. Furthermore, a plurality of gate **trenches** are provided at a specific pitch while the other **insulating layers** 15 are provided on the positions held by the gate **trenches** of the **semiconductor** substrate 1

36/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014397778
WPI Acc No: 2002-218481/200228
Related WPI Acc No: 1995-285002
XRAM Acc No: C02-067020
XRPX Acc No: N02-167520

Insulated gate **semiconductor device** e.g., metal oxide **semiconductor** transistor having **trench** gate includes first **main electrode** and second and third **semiconductor** layers which are connected through a platinum silicide **conductive layer**

Patent Assignee: MITSUBISHI DENKI KK (MITQ)
Inventor: HARADA M; MINATO T; NISHIHARA H; TAKAHASHI H
Number of Countries: 003 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1120834	A2	20010801	EP 95101793	A	19950209	200228	B
			EP 2001108780	A	19950209		

Priority Applications (No Type Date): JP 9422459 A 19940221
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1120834	A2	E	65	H01L-029/45	Div ex application EP 95101793 Div ex patent EP 668616

Designated States (Regional): DE FR GB

Abstract (Basic): EP 1120834 A2
Abstract (Basic):

NOVELTY - Insulated gate **semiconductor device** includes a first **main electrode** (212) and second (205) and third (206) **semiconductor** layers which are electrically connected through a platinum silicide **conductive layer**.

DETAILED DESCRIPTION - Insulated gate **semiconductor device** includes a **semiconductor** base body with upper and lower main surfaces. The **semiconductor** base body comprises: first (204) and third (206) **semiconductor layers** of first **conductivity** type with a second **semiconductor layer** (205) of second **conductivity** type between these **layers**. A set of **trenches** (207) are formed in a stripe along the upper main surface the **semiconductor** base body and extend into the first **semiconductor layer**. A gate **insulating film** (209) and a gate **electrode** (210) are formed in each **trench**. The second and third **semiconductor** layers are selectively exposed in the upper main surface interposed between adjacent **trenches**. A first **main electrode** (212) is electrically connected to both the second and third **semiconductor** layers on the upper main surface and insulated from the gate **electrode**. A second **main electrode** is electrically connected to the lower main surface. A platinum silicide **conductive layer** is interposed between the first **main electrode** and the upper **main**

surface. The first **main electrode** and the second and third **semiconductor** layers are electrically connected through the **conductive layer**.

USE - Insulator gate **semiconductor device** e.g., metal oxide **semiconductor** transistor having **trench** gate (UMOS), UMOS - insulator **gate bipolar transistor** (UMOS - **IGBT**), emitter switched thyristor (EST) and metal oxide **semiconductor** controlled thyristor (MCT).

ADVANTAGE - Contact resistance between the third **semiconductor** layer and the first **electrode** is decreased. Therefore ON voltage does not increase even if the contact area of the third **semiconductor** layer and the first **main electrode** is decreased due to miniaturization. The device effectively makes use of miniaturization to decrease the ON voltage.

DESCRIPTION OF DRAWING(S) - The diagram shows a cross-sectional perspective view of a UMOS - **IGBT**.

UMOS - **IGBT** (110)
P+ collector layer (202)
N+ buffer collector layer (203)
N- **semiconductor** layer (first **semiconductor** layer) (204)
P base layer (second **semiconductor** layer) (205)
N+ emitter layer (third **semiconductor** layer) (206)
Trench (207)
Channel region (208)
Gate **insulating film** (209)
Gate **electrode** (210)
Emitter **electrode** (first **main electrode**) (212)
Collector **electrode** (213)
pp; 65 DwgNo 1/45

09/04/2002 09/986,277

36/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013959329
WPI Acc No: 2001-443543/200148
XRPX Acc No: N01-328147
Semiconductor device with **trench** gate, such as insulated- **gate bipolar transistor** comprises first **semiconductor layer** of first **conductivity**
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: INOUE T; NINOMIYA H; OGURA T; SUGIYAMA K
Number of Countries: 026 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1089343	A2	20010404	EP 2000308599	A	20000929	200148	B
JP 2001102579	A	20010413	JP 99280046	A	19990930	200148	
JP 2001168333	A	20010622	JP 2000294986	A	20000927	200151	

Priority Applications (No Type Date): JP 99280046 A 19990930; JP 99278254 A 19990930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1089343	A2	E	28	H01L-029/739	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
JP 2001102579	A		6	H01L-029/78	
JP 2001168333	A		15	H01L-029/78	

Abstract (Basic): EP 1089343 A2
Abstract (Basic):
NOVELTY - In the insulated-**gate bipolar transistor** (**IGBT**), a p-base layer (12) is formed on an n-base layer (11). A number of main **trenches** (13) are formed as stripes to extend through the p-base layer. A pair of n-emitter layers (15) are formed in the p-base layer between a pair of main **trenches**. An **insulating film** (18) is selectively formed on the p-base layer, n-emitter layers, and **main trenches**. An emitter **electrode** (19) is formed on the **insulating film**. A p-emitter layer (17) is formed opposite-side surface of the n-base layer via an n-buffer layer (16). Between the n-emitter layers in the current path region (41), a narrowing **trench** (22) is formed to extend through the p-base layer from its surface and reach the n-base layer.
DETAILED DESCRIPTION - The narrowing **trench** narrows a hole flow path formed from the n-base layer to the emitter **electrode** through the p-base layer.
USE - None given.
ADVANTAGE - The **semiconductor device** can increase the hole flow resistance without reducing the distance between **trenches** and decrease the **conduction** loss. The devices also reduces the gate-collector capacitance without increasing the **conduction** loss.
DESCRIPTION OF DRAWING(S) - The drawing is a sectional view showing

the main part of an **IGBT** as a **semiconductor device** with a **trench** gate.
N-base layer (11)
P-base layer (12)
Main **trenches** (12)
N-emitter layers (15)
N-buffer layer (16)
P- emitter layer (17)
Insulating film (18)
Emitter **electrode** (19)
Narrowing **trench** (22)
Current path region (41)
pp; 28 DwgNo 1/27

36/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012056370
WPI Acc No: 1998-473281/199841
XRPX Acc No: N98-369583
Voltage driven **semiconductor device** with **trench** type insulated gate **electrode** - has pair of **insulating films**, one among which adjoins insulated gate **electrode** and another **insulating film** on Si substrate
Patent Assignee: HITACHI LTD (HITA)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10200104	A	19980731	JP 973588	A	19970113	199841	B

Priority Applications (No Type Date): JP 973588 A 19970113
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10200104	A		8	H01L-029/78	

Abstract (Basic): JP 10200104 A
The device has a first conductivity type second **semiconductor** area which adjoins a first **semiconductor** area formed on a P+ Si substrate (1). A second conductivity type third **semiconductor** area is formed adjoining the second **semiconductor** area. A first conductivity type fourth **semiconductor** area is formed in the third **semiconductor** area.
A pair of **main electrodes** are connected to the first and fourth **semiconductor** areas respectively. A set of insulated gate **electrodes** are arranged in several **trenches** individually penetrating into the third **semiconductor** area. An **insulating film** (7) thicker than that of gate **electrode** is formed adjoining the third **semiconductor** area. Another **insulating film** (8) adjoins the gate **electrode** and the first **insulating film**.
USE - For e.g. power MOSFET, **IGBT**.
ADVANTAGE - Stabilises threshold voltage. Secures desired gate breakdown voltage. Prevents latch up of parasitic thyristor.
Dwg.1/9

36/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010402021
WPI Acc No: 1995-303334/199540
XRPX Acc No: N95-230430
Semiconductor device e.g. **IGBT** - has several trough parts selectively formed to preset depth from first main surface
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: MINATO T; NAKAMURA K; SHIOZAWA K; TOMINAGA S
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 19506386	A1	19950831	DE 1006386	A	19950223	199540	B
NL 9500370	A	19951002	NL 95370	A	19950224	199544	
JP 7235676	A	19950905	JP 9426874	A	19940224	199546	
US 5508534	A	19960416	US 95384734	A	19950207	199621	
US 5578522	A	19961126	US 95384734	A	19950207	199702	
			US 95565277	A	19951130		

Priority Applications (No Type Date): JP 9426874 A 19940224
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19506386	A1		38	H01L-029/739	
JP 7235676	A		20	H01L-029/78	
US 5508534	A		23	H01L-027/02	
US 5578522	A		23	H01L-021/44	Div ex application US 95384734 Div ex patent US 5508534
NL 9500370	A			H01L-029/739	

Abstract (Basic): DE 19506386 A
On the inner walls of the trough parts are formed **insulating layers**. The trough parts are filled with **control electrode** layers, sandwiching with the trough part inner walls the **insulating layers**. The **control electrode layers** are covered by **insulating layer** extending from the first main surface.
Over the first main surface is formed a first **main electrode**, with the second one on the second main surface. A control voltage, applied to the **control electrode** layers, controls the current between the two **main electrodes**. The **insulating layers** have a slightly inclined surface from tip to bottom, meeting a specified formula related to the surface length and height.
USE/ADVANTAGE - For power MOSFET, **IGBT**, GTO and MOS-gate thyristors, with increased **electrode** wiring thickness even layer formation, and flat wiring layer.
Dwg.1/28
Abstract (Equivalent): US 5578522 A
A **method of** fabricating a **semiconductor device**, comprising the steps of:

(a) providing a body of **semiconductor** having first and second major surfaces;

(b) selectively forming a plurality of **trench** portions extending from the first major surface of said body to a predetermined depth;

(c) forming a **plurality** of **control electrode** layers filling said plurality of **trench** portions, respectively, and extending over part of the first major surface of said body, the operation of said device being controlled by a control voltage applied commonly to said plurality of **control electrode** layers after completion of said device;

(d) forming an **insulating layer** on the first major surface of said body including said plurality of **control electrode** layers;

(e) patterning said **insulating layer** to form an opening in a predetermined position; and

(f) performing heat treatment upon said patterned **insulating layer** to form a smooth inclined surface adjacent said opening of said **insulating layer**,

wherein the heat treatment in said step (f) is carried out above a temperature at which said **insulating layer** is softened.

Dwg.9,10/2

8

US 5508534 A

A **semiconductor device** comprising:

a **semiconductor** body having first and second major surfaces;

a plurality of **trench** portions each selectively formed in the first major surface of said body to a predetermined depth;

a plurality of **insulating films** formed on respective inner walls of said plurality of **trench** portions;

a plurality of **control electrode** layers filled respectively in said plurality of **trench** portions, with said plurality of **insulating films** sandwiched between said **control electrode** layers and the inner walls of said **trench** portions;

a plurality of **insulating layers** formed respectively on said plurality of **control electrode** layers and projecting from the first major surface of said body;

a first **main electrode** formed over the first major surface of said body; and

a second **main electrode** formed on the second major surface of said body,

wherein a control voltage applied commonly to said plurality of **control electrode** layers controls current between said first and second **main electrodes**, and

wherein each of said plurality of **insulating layers** has an opposite surface, which is opposite the first surface, with rounded edges between an inclined surface, extending from the first major surface, and said opposite surface for preventing cavities from forming in the first **main electrode** during formation of the **semiconductor device**, and

the conditional expression: Y/Xat most5 is satisfied where X is a length of said rounded edges in a direction of the first major surface

of said body and Y is a height measured between a point where the rounded edges meet the opposite surface and the first major surface of said body.

Dwg.1/28

36/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008997759
WPI Acc No: 1992-125031/199216
XRAM Acc No: C92-058315
XRPX Acc No: N92-093500
Insulated gate bipolar **semiconductor device** - in which on-voltage is low even under conditions of high speed and high withstand voltage
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: HAGINO H
Number of Countries: 005 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 480356	A	19920415	EP 91117060	A	19911007	199216	B
JP 4146674	A	19920520	JP 90270733	A	19901008	199227	
EP 480356	A3	19920520	EP 91117060	A	19911007	199331	
US 5304821	A	19940419	US 91767480	A	19910930	199415	
US 5380670	A	19950110	US 91767480	A	19910930	199508	
			US 94190494	A	19940202		
EP 480356	B1	19950308	EP 91117060	A	19911007	199514	
DE 69107949	E	19950413	DE 607949	A	19911007	199520	
			EP 91117060	A	19911007		

Priority Applications (No Type Date): JP 90270733 A 19901008
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 480356	A	E	18		
Designated States (Regional): DE FR SE					
JP 4146674	A		9	H01L-029/784	
US 5304821	A		15	H01L-029/74	
US 5380670	A		16	H01L-021/265	Div ex application US 91767480 Div ex patent US 5304821
EP 480356	B1	E	23	H01L-029/74	
Designated States (Regional): DE FR SE					
DE 69107949	E			H01L-029/74	Based on patent EP 480356

Abstract (Basic): EP 480356 A

A **semiconductor device** comprises a first **semiconductor layer** of a first **conductivity** type having upper and lower major surfaces; a second **semiconductor layer** of a second **conductivity** type formed on the upper major surface of the first layer; a third **semiconductor layer** of the first **conductivity** type formed in a top surface of the second layer; at least one fourth **semiconductor layer** of the second **conductivity** selectively formed and buried in the third layer; at least one fifth **semiconductor layer** of the second **conductivity** type selectively formed in a top surface of the third layer, and being displaced above the fourth layer, wherein at least on **trench** extending from a top surface of

the fifth layer is formed into the fourth layer through the third and fifth **layers**; an **insulating layer** formed on an inner wall of the **trench**; a **control electrode** formed on the **insulating layer** in the **trench**; a first **main electrode** layer being in contact with both the top surface of the third layer and the top surface of the fifth layer; and a second **main electrode** layer formed on the lower major surface of the first layer.

USE/ADVANTAGE - **IGBT** in which ON-voltage is low even on the conditions of a high speed and a high withstand voltage.

Dwg.1G/6

Abstract (Equivalent): EP 480356 B

A **semiconductor device** comprises a first **semiconductor layer** of a first **conductivity** type having upper and lower major surfaces; a second **semiconductor layer** of a second **conductivity** type formed on the upper major surface of the first layer; a third **semiconductor layer** of the first **conductivity** type formed in a top surface of the second layer; at least one fourth **semiconductor layer** of the second **conductivity** selectively formed and buried in the third layer; at least one fifth **semiconductor layer** of the second **conductivity** type selectively formed in a top surface of the third layer, and being displaced above the fourth layer, wherein at least on **trench** extending from a top surface of the fifth layer is formed into the fourth layer through the third and fifth **layers**; an **insulating layer** formed on an inner wall of the **trench**; a **control electrode** formed on the **insulating layer** in the **trench**; a first **main electrode** layer being in contact with both the top surface of the third layer and the top surface of the fifth layer; and a second **main electrode** layer formed on the lower major surface of the first layer.

USE/ADVANTAGE - **IGBT** in which ON-voltage is low even on the conditions of a high speed and a high withstand voltage.

EP-480356 A **semiconductor device** comprising: a first **semiconductor** layer (1) of a first conductivity type having upper and lower major surfaces; a second **semiconductor** layer (2, 3) of a second conductivity type formed on said upper major surface of said first **semiconductor** layer; a third **semiconductor** layer (4a, 4b) of the first conductivity type formed in a top surface of said second **semiconductor** layer; at least one fourth **semiconductor** layer (5b) of the second conductivity selectively formed and buried in said third **semiconductor** layer; at least one fifth **semiconductor** layer (5a) of the second conductivity type selectively formed in a top surface of said third **semiconductor** layer, said fifth **semiconductor** layer being positioned above said fourth **semiconductor** layer, wherein at least one **trench** (13) is formed extending from a top surface of said fifth **semiconductor** layer into said fourth **semiconductor** layer through said third and fifth **semiconductor layers**; an **insulating layer** (7a) formed on an inner wall of said **trench**; a **control electrode** (8a) formed on said **insulating layer** in said **trench**; a first **main electrode** layer (9a) being in contact with both said top surface

of said third **semiconductor** layer and said top surface of said fifth **semiconductor** layer; and a second **main electrode** layer (10) formed on said lower major surface of said first **semiconductor** layer.

(Dwg.1G/6

Abstract (Equivalent): US 5380670 A

The **semiconductor device** is mfd. by (a) forming a 1st part of a 2nd 2nd-type **semiconductor** layer on an upper major surface of a 1st 1st-type **semiconductor** layer, (b) forming a 1st part of a 3rd 1st-type layer in a top surface of the 1st part of the 2nd **semiconductor** layer, (c) selectively forming at least one 4th 2nd-type in a top surface of the 1st part of the 3rd layer, (d) forming a 2nd part of the 3rd layer on respective top surfaces of the 1st part of the 3rd and 4th layers, (e) selectively forming at least one 2nd-type 5th layer in a top surface of the 2nd part of the 3rd layer, the 5th layer being located above the 4th layer, (f) forming **trench**(es) extending from a top of the 5th layer into the 4th layer through the 5th layer and 2nd part of the 3rd **layer**, (g) forming an **insulating layer** and a **control electrode** on the **trench** inner wall, (h) forming a 1st **main electrode** layer contacting the top surface of the 2nd part of the 3rd layer and top of the 5th layer, and (i) forming a 2nd **main electrode** layer on the lower major surface of the 1st **semiconductor** layer.

ADVANTAGE - Reduced ON voltage without a redn. in withstand voltage.

Dwg.1g/6

US 5304821 A

The device comprises (a) a 1st **conductivity** type 1st **semiconductor layer**, (b) a 2nd type 2nd **semiconductor** layer formed on the upper major surface of the 1st layer, (c) a 1st type 3rd layer formed in a top surface of the 2nd layer, (d) at least one 2nd type 4th **semiconductor** layer buried in the 3rd layer, (e) at least one 2nd type 5th **semiconductor** layer formed in a top surfac eof the 3rd layer and is placed above the 4th **layer**, (f) an **insulating layer** on an inner wall of a **trench** extending from the top of the 5th layer to the 4th layer through the 3rd and 5th layers, (g) a **control electrode** on the **insulating layer**, (h) a 1st **main electrode** layer in contact with both the top of the 3rd and top of the 5th layers, and (i) a 2nd **main electrode** on the lower major surface of the 1st layer.

ADVANTAGE - The ON-voltage is low even at high speed and high with stand voltage.

Dwg.1/6

36/3,AB/6 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05318851
DIELECTRIC ISOLATION **SEMICONDUCTOR DEVICE** AND ITS MANUFACTURE

PUB. NO.: 08-274351 [JP 8274351 A]
PUBLISHED: October 18, 1996 (19961018)
INVENTOR(s): ENDO KOICHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-073344 [JP 9573344]
FILED: March 30, 1995 (19950330)

ABSTRACT

PURPOSE: To obtain a diode, an **IGBT** or the like which can realize a high-speed switching operation and whose structure is new without using a carrier life control technique by specifying the width of a part sandwiched between element isolation **insulating films** in a current route formed between a first **main electrode** and a second **main electrode**.

CONSTITUTION: The mutual distance W between one pair of **trench** sidewall **insulating films** 1 along a current route is set at 5.mu.m or lower. Since it is difficult to work the thickness (t) of a substrate to be thin considering a breakdown strength, an element whose width W is made thin in the transverse direction is formed. That is to say, the mutual distance W between the pair of **trench** sidewall **insulating films** 1 along the current route is made small with reference to the thickness (t) of an active layer and the distance (l) between both **electrodes**. As a result, the effective area of a **semiconductor** element such as a diode or the like can be suppressed small, and the reverse recovery charge of the diode can be reduced. Consequently, a **semiconductor device** such as a high-speed diode, a high-speed **IGBT** or the like can be realized without controlling a lifetime.

38/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014463036
WPI Acc No: 2002-283739/200233
XRAM Acc No: C02-083391
XRPX Acc No: N02-221596

Semiconductor device, e.g. insulated gate type bipolar transistor, power MOSFET, electrically connects gate **electrode** formed within **trench** and source base **electrode**

Patent Assignee: TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001203356	A	20010727	JP 200012103	A	20000120	200233	B

Priority Applications (No Type Date): JP 200012103 A 20000120
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001203356	A		8	H01L-029/78	

Abstract (Basic): JP 2001203356 A
Abstract (Basic):

NOVELTY - A N-type source area (13) is selectively formed on P-type base region (12) of substrate. **Trenches** are formed on base region whose inner wall is **coated** with gate **insulating film** (14). A **layer insulating film** (16) is formed above the substrate. A connection portion (21) electrically connects a gate **electrode** (15) which is embedded in the **trench** and a source-base **electrode** (17) which is formed on the source and base region through contact hole.

USE - E.g. insulated gate type bipolar transistor (**IGBT**), power metal oxide **semiconductor** field effect transistor (MOSFET), MOS control type thyristor (MCT), injection enhanced gate transistor (IEGT).

ADVANTAGE - As the gate **electrode** is formed in the **trench** the **gate capacitance** and switch loss is reduced. Also the ON resistance is maintained, as a flat surface pattern of **trench** gate is formed.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of **semiconductor device**.

P-type base region (12)
N-type source area (13)
Gate **insulating film** (14)
Gate **electrode** (15)
Layer insulating film (16)
Source base **electrode** (17)
Connection portion (21)
pp; 8 DwgNo 1/12

38/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013598161
WPI Acc No: 2001-082368/200110
XRPX Acc No: N01-062883
A **trench** insulating gate type bipolar transistor (**IGBT**) **semiconductor** for a power converter includes **trench** insulating gate **electrodes** and has a p-type well layer as deep as the **electrodes** in a wide interval between the **electrodes**
Patent Assignee: HITACHI LTD (HITA)
Inventor: MORI M; OYAMA K; SAKANO J
Number of Countries: 027 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1032047	A2	20000830	EP 2000301097	A	20000211	200110	B
JP 2000307116	A	20001102	JP 200045081	A	20000217	200110	
KR 2000076628	A	20001226	KR 20005888	A	20000209	200134	

Priority Applications (No Type Date): JP 9938166 A 19990217
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1032047	A2	E	26	H01L-029/739	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI				
JP 2000307116	A		15	H01L-029/78	
KR 2000076628	A			H01L-029/73	

Abstract (Basic): EP 1032047 A2
Abstract (Basic):
NOVELTY - An n-type base layer (1) has a cathode (C) **electrode** (11) on a p-type collector layer (2) on a buffer layer (3) and an emitter (E) **electrode** (10) on a p-type base **layer** (4). **Trench insulating** gate **electrodes** (7) are formed so deep that they reach the base layer. In a narrow interval (La) between gate **electrodes**, a p+ layer (6) is formed across and deeper than an n-type source layer (5). In a wide interval (Lb), a p-type well layer (9) is formed as deep as the **trench** gate **electrodes**.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a power converter using a **trench IGBT**.
USE - The **trench** insulating gate type bipolar transistor (**IGBT**) **semiconductor** is used for a power converter.
ADVANTAGE - The **semiconductor** is able to withstand a higher voltage whilst reducing the **gate** input **capacity**, switching loss and drive power. It enables the reliability and efficiency of a power converter to be improved.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a **trench IGBT**.
Base layer (1)
Collector layer (2)
Buffer layer (3)

Base layer (4)
Source layer (5)
p+ layer (6)
Gate **electrode** (7)
p-type well layer (9)
Cathode **electrode** (10)
Emitter **electrode** (11)
pp; 26 DwgNo 1/16

38/3,AB/3 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06975785
SEMICONDUCTOR DEVICE

PUB. NO.: 2001-203356 [JP 2001203356 A]
PUBLISHED: July 27, 2001 (20010727)
INVENTOR(s): KOBAYASHI MASAKAZU
NAKANISHI HIDETOSHI
APPLICANT(s): TOSHIBA CORP
APPL. NO.: 2000-012103 [JP 200012103]
FILED: January 20, 2000 (20000120)

ABSTRACT

PROBLEM TO BE SOLVED: To maintain the on-resistance of a **trench** **IGBT** equivalent to that of the conventional planar gate structure and reduce the **gate capacitance** and the switch loss to make it adapted to the high frequency use.

SOLUTION: The device comprises P+ base regions 12 formed on surface layers of N- layer collector regions 11, N+ source regions 13 selectively formed on surface **layers** thereof, a gate **insulating film** 14 formed on inner walls of **trenches** , a substrate surface, and a plurality of rows of intermittent stripe plane patterns in source regions. Further, the device is formed down to a depth to pierce base regions, **trench** gate **electrodes** 15 buried in the **trenches**, **layer** **insulation** **film** 16, surface emitter **electrodes** 17 commonly contacting to the source regions and the base regions through openings of the **layer insulation film** and its lower **layer** gate **insulation** **film**, and connecting parts 21 for electrically connecting **trench** gate **electrodes** buried in the **trenches**.

42/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009353402
WPI Acc No: 1993-046881/199306
XRPX Acc No: N93-035918
Lateral **trench-gate bipolar transistor** for power applications - has vertical insulated gate regions adjacent channel regions which partly surround second device regions to induce vertical induction channel during operation
Patent Assignee: PHILIPS ELECTRONICS NV (PHIG); PHILIPS GLOEILAMPENFAB NV (PHIG); KONINK PHILIPS ELECTRONICS NV (PHIG); NORTH AMERICAN PHILIPS CORP (PHIG)
Inventor: SIN J K O
Number of Countries: 008 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 526939	A1	19930210	EP 92202313	A	19920728	199306	B
US 5227653	A	19930713	US 91741288	A	19910807	199329	
JP 5206159	A	19930813	JP 92208104	A	19920804	199337	
EP 526939	B1	19960501	EP 92202313	A	19920728	199622	
DE 69210328	E	19960605	DE 610328	A	19920728	199628	
			EP 92202313	A	19920728		
KR 278526	B	20010201	KR 9214158	A	19920807	200210	

Priority Applications (No Type Date): US 91741288 A 19910807
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 526939	A1	E	7	H01L-029/72	
Designated States (Regional): DE FR GB IT NL					
US 5227653	A		5	H01L-029/00	
JP 5206159	A			H01L-021/331	
EP 526939	B1	E	9	H01L-029/739	
Designated States (Regional): DE FR GB IT NL					
DE 69210328	E			H01L-029/739	Based on patent EP 526939
KR 278526	B			H01L-029/70	Previous Publ. patent KR 93005238

Abstract (Basic): EP 526939 A
The transistor has spaced-apart, surface adjoining, two device regions (24), a surface adjoining channel region (22), and a gate region (20) adjacent to, but insulated from the second device region and the channel region.
The gate region extends in a vertical direction adjacent the second device region and the second channel region and induces a substantially vertical **conduction** channel in the channel region during operation.
ADVANTAGE - Low on-resistance, fast switching speed, high breakdown voltage and high latch-up current density.
Dwg.1/2
Abstract (Equivalent): EP 526939 B
A **semiconductor** lateral insulated **gate bipolar transistor** device (1) comprising a **semiconductor** substrate (10) of a first conductivity type having a major surface (12); a

semiconductor surface layer (14) of a second conductivity type opposite that of the first located on the said major surface (12), a **trench** (16) extending entirely through said surface layer (14), surrounding a portion of said surface layer (14) thereby defining an island in said surface layer (14), and having an inner sidewall, an outer sidewall and a floor, the inner sidewall bounding said island, a **dielectric layer** (18) covering the sidewalls and floor of said **trench** (16), a gate region (20) lying within said **trench** on said **dielectric layer** (18) and comprising a **conductive** material, a surface-adjoining channel region (22) of said first conductivity type located in said island of said surface layer (14) and adjoining said inner sidewall of said **trench** (16), a surface-adjoining first device region (26) located in a central portion of said island of said surface layer (14) and spaced apart from said channel region (22), a surface-adjoining second device region (24a,24b) located in said channel region (22) and comprising at least a highly-doped surface-adjoining zone (24a) of said second conductivity type adjacent said inner sidewall of said **trench** (16), an **electrode** (A) providing an electrical connection to said first device region (26), and an **electrode** (A) providing an electrical connection to said second device region (24a,24b), said gate region (20) extending in a substantially vertical direction adjacent said second device region (24a,24b) and said channel region (22), whereby a substantially vertical **conduction** channel is induced in the channel region (22) during operation.

(Dwg.1/2

Abstract (Equivalent): US 5227653 A

The lateral **trench-gate bipolar transistor** device includes spaced-apart, surface-adjoining, laterally-oriented anode and cathode **regions**. A channel **region partially** surrounds the cathode **region**, and a gate region is provided adjacent to, but insulated from, the cathode region and the channel region. The gate region extends in a vertical direction adjacent the cathode region and the channel region in order to induce a substantially vertical **conduction** channel in the channel region of the lateral device during operation.

The gate region can advantageously be provided in a **trench** surrounding the transistor device, with a **trench**-shaped gate **dielectric layer** being provided on the **trench** sidewalls and floor to insulate the gate from the remainder of the device. Devices may be fabricated in an epitaxial surface layer, which may be provided either directly on a **semiconductor** substrate, or else on an intervening **insulating layer**. These devices provide the advantages of low on-resistance, fast switching speed, high breakdown voltage and high latch up current density.

USE/ADVANTAGE - for MOS field-effect device, partic. LTGBT used in power IC applications. Improved resistance to latch-up in high power or high voltage circuit applications. Fast switching characteristics.

(Dwg.2/2

43/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014583913
WPI Acc No: 2002-404617/200243
XRPX Acc No: N02-317618
Trench insulated **gate bipolar transistor** has **insulating layer** in **trench** that acts as gate isolation film only in region required for MOS channel to function
Patent Assignee: INFINEON TECHNOLOGIES AG (INFN)
Inventor: PFIRSCH F
Number of Countries: 094 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200219434	A1	20020307	WO 2000EP8459	A	20000830	200243	B
AU 200074149	A	20020313	AU 200074149	A	20000830	200249	
			WO 2000EP8459	A	20000830		

Priority Applications (No Type Date): WO 2000EP8459 A 20000830
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200219434	A1	G	26	H01L-029/739	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TZ UG ZW

AU 200074149 A H01L-029/739 Based on patent WO 200219434

Abstract (Basic): WO 200219434 A1
Abstract (Basic):

NOVELTY - The device has an insulated **trench** (5) extending from a first main surface to a second base zone and containing an active MOS channel and emitter and collector contacts (11,13). The **insulating layer** (7,17) in the **trench** acts as a gate isolation film only in the area required for the MOS channel to function.

DETAILED DESCRIPTION - The device has an emitter zone (4) of a first **conductor** type bounding on a first main surface (9) of a **semiconducting** body (1-4), a base zone around the emitter zone of a second opposite **conductor** type, a second base zone of the first **conductor** type, a collector zone (1) of the second **conductor** type forming a second main surface (12), a gate **electrode** (8) in an insulated **trench** (5) extending from the first man surface to the second base zone and containing an active MOS channel and emitter and collector contacts (11,13). The **insulating layer** (7,17) in the **trench** acts as a gate isolation film only in the area required for the MOS channel to function.

USE - **Trench** insulated **gate bipolar transistor**.

ADVANTAGE - Feedback capacitance is reduced in simple manner

without increasing the gate resistance.
DESCRIPTION OF DRAWING(S) - The drawing shows a schematic representation of a **trench** insulated **gate bipolar transistor**
emitter zone (4)
main surfaces (9,12)
semiconducting body (1-4)
collector zone (1)
gate **electrode** (8)
trench (5)
emitter and collector contacts (11,13)
insulating layers (7,17)
pp; 26 DwgNo 1/9

43/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014578869
WPI Acc No: 2002-399573/200243
XRAM Acc No: C02-112803
XRPX Acc No: N02-313415
Trench gate type **semiconductor device** for drive control of motor, has **insulation film** which consists of borophosphosilicate glass including specified amount of oxidation boron and phosphorus pentoxide
Patent Assignee: FUJI ELECTRIC CO LTD (FJIE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2002076342	A	20020315	JP 2000268461	A	20000905	200243	B

Priority Applications (No Type Date): JP 2000268461 A 20000905
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2002076342	A		4	H01L-029/78	

Abstract (Basic): JP 2002076342 A
Abstract (Basic):
NOVELTY - An **insulation film** (7) which consists of a boron phosphorus silica glass having sum of oxidation boron and phosphorus pentoxide in the range of the 8-15 mol.%, covers a gate **electrode** (6) formed through a thin gate oxide film (5) in the **trench** (11).
USE - **Trench** gate type **semiconductor device** such as MOSFET, insulated **gate bipolar transistor** (**IGBT**) and voltage drive type thyristor used for drive control of motor.
ADVANTAGE - As the sum of oxidation boron and the phosphorus silica glass included in the boron phosphorus silica glass is in the specific range, the degradation of property due to foreign materials such as resist is suppressed, improvement in patterning accuracy, etching variation reduction and sheet resistance reduction of source **electrode**, improvement in reliable film formation and reduction in damage of wire bonding at the time of assembly, are achieved.
DESCRIPTION OF DRAWING(S) - The figure shows the vertical sectional view of the MOSFET. (Drawing includes non-English language text).
Thin gate oxide film (5)
Gate **electrode** (6)
Insulation film (7)
Trench (11)
pp; 4 DwgNo 1/3

43/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014419054
WPI Acc No: 2002-239757/200229
XRPX Acc No: N02-184928
Trench gate **semiconductor devices** e.g. insulated gate field effect transistor, has gate **electrode** formed contacting gate material on whole area of **trenches**
Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG); PHILIPS CORP (PHIG)
Inventor: WARWICK A M
Number of Countries: 022 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200169685	A2	20010920	WO 2001EP2416	A	20010305	200229 B
US 20010023957	A1	20010927	US 2001808277	A	20010314	200229
EP 1198842	A2	20020424	EP 2001923628	A	20010305	200235
			WO 2001EP2416	A	20010305	

Priority Applications (No Type Date): GB 20006092 A 20000315
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200169685	A2	E	27	H01L-029/78	
				Designated States (National): JP	
				Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR	
US 20010023957	A1			H01L-029/76	
EP 1198842	A2	E		H01L-029/78	Based on patent WO 200169685
				Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR	

Abstract (Basic): WO 200169685 A2
Abstract (Basic):
NOVELTY - Active cell area has several **trenches** (20) with gate material (21) and adjacent to each **trench**, source region (13A) is formed. The **trenches** with gate material, extend beyond the active area to inactive area. On each inactive area, gate **electrode** (53) is formed contacting gate material on whole area of the **trenches**.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **trench** gate **semiconductor device** manufacturing method.
USE - E.g. insulated gate field effect transistor, insulated **gate bipolar transistor**.
ADVANTAGE - As gate **electrode** contacts gate material on whole area of the **trenches**, an improved contact with gate material is provided with small **trench** width. As the whole area of **trench** extends beyond the active cell area to inactive area, the **insulating layer** breakdown voltage is reduced.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of **trench** gate **semiconductor device**.
Source region (13A)

09/04/2002 09/986,277

Trenches (20)
Gate material (21)
Gate **electrode** (53)
pp; 27 DwgNo 4/9

43/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014408952
WPI Acc No: 2002-229655/200229
Related WPI Acc No: 1995-270686; 2002-141577
XRPX Acc No: N02-176629
Semiconductor device e.g. MOSFET has **trench** extending in thickness direction of substrate, which has rounded opening
Patent Assignee: MITSUBISHI DENKI KK (MITQ)
Inventor: MINATO T; NAKAMURA K; SHIOZAWA K; TOMINAGA S
Number of Countries: 004 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1160872	A2	20011205	EP 95101591	A	19950206	200229 B
			EP 2001121361	A	19950206	

Priority Applications (No Type Date): JP 951347 A 19950109; JP 9412559 A 19940204
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1160872	A2	E	75	H01L-029/423	Div ex application EP 95101591 Div ex patent EP 666590

Designated States (Regional): DE FR GB NL

Abstract (Basic): EP 1160872 A2
Abstract (Basic):
NOVELTY - The device has a **trench** extending in the thickness direction of a **semiconductor** substrate (1). The **trench** is filled with a predetermined material to form a gate **electrode** (22). The opening (5e) of the **trench** is rounded.
USE - E.g. metal oxide **semiconductor** field effect transistor (MOSFET), insulated **gate bipolar transistor** (**IGBT**), MOS controlled thyristor (MCT).
ADVANTAGE - Since the opening of the **trench** is rounded, the defects near the **trench** are reduced, alleviating the electric field concentration at the edges, enhancing uniform electric field distribution.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the **semiconductor device**.
Substrate (1)
Opening (5e)
Gate **electrode** (22)
pp; 75 DwgNo 5A/81

43/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014342866
WPI Acc No: 2002-163569/200221
XRPX Acc No: N02-124860
Semiconductor device e.g. field effect transistor has **dielectric layer** with greater thickness in **trench** portion extending into drain drift region, so that field plate is formed by extension of gate **conductive** region
Patent Assignee: HIJZEN E A (HIJZ-I); HUETING R J E (HUET-I); KONINK PHILIPS ELECTRONICS NV (PHIG)
Inventor: HIJZEN E A; HUETING R J E
Number of Countries: 021 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010045599	A1	20011129	US 2001860358	A	20010518	200221 B
WO 200191190	A1	20011129	WO 2001EP4932	A	20010501	200221

Priority Applications (No Type Date): GB 200012138 A 20000520
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010045599	A1		11	H01L-029/76	
WO 200191190	A1	E		H01L-029/78	

Designated States (National): JP
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

Abstract (Basic): US 20010045599 A1
Abstract (Basic):
NOVELTY - A **trench** in which insulated gate is provided, extends from main region to drain drift region. A gate **conductive** region (70b) is separated from the **trench** by a **dielectric layer** (71a). The **dielectric layer** has greater thickness in **trench** portion extending into drain drift region than in remaining portions, so that field plate is formed by extension of gate **conductive** region towards drain region (5).
USE - **Semiconductor device** e.g. field effect transistor, insulated gate field effect **device**, metal **semiconductor** field effect transistor, insulated **gate bipolar transistor**, Schottky source devices.
ADVANTAGE - Improves current carrying capabilities. Provides low on-resistance. Withstands high voltage between source and drain regions, when the field effect transistor is non-**conducting**.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of field effect transistor.
Drain region (5)
Gate **conductive** region (70b)
Dielectric layer (71a)
pp; 11 DwgNo 2/10

43/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014311852
WPI Acc No: 2002-132554/200218
Related WPI Acc No: 1997-344410; 2001-302463; 2002-132550; 2002-132551; 2002-132552; 2002-132553
XRPX Acc No: N02-100011

Semiconductor device such as MOSFET, **IGBT**, **bipolar transistor**, and **semiconductor** diode has gate **electrode** disposed in **trench**, and provided in contact with first **conductive** type source region

Patent Assignee: FUJI ELECTRIC CO LTD (FJIE)
Inventor: FUJIHIRA T
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2355588	A	20010425	GB 971204	A	19970121	200218	B
			GB 20011052	A	20010115		

Priority Applications (No Type Date): JP 967935 A 19960122
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2355588	A		72	H01L-029/78	Derived from application GB 971204

Abstract (Basic): GB 2355588 A
Abstract (Basic):

NOVELTY - A first **conductive** type source region (18) is spaced apart from a first **conductive** type drift path region (14) via the second **conductive** type well. A gate **electrode** (11) is disposed in a **trench**, and provided in contact with the first **conductive** type source region (18) and the second **conductive** type well via a gate **insulation film**. The gate **electrode** extends deeper than the second **conductive** type **layer**.

USE - drift path region 14

ADVANTAGE - Relaxes the relationship between the ON resistance and the breakdown voltage to enable an increase in the current capacity by a reduction in the ON resistance under the high breakdown voltage

DESCRIPTION OF DRAWING(S) - The drawing is a cross-sectional view showing a p-channel vertically structured MOSFET of the present invention.

source region (18)
drift path region (14)
pp; 72 DwgNo 10/12

43/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014297553
WPI Acc No: 2002-118256/200216
XRPX Acc No: N02-088523
Semiconductor device e.g. bidirectional **IGBT** for electric power converter, has gate **insulating films** and gate **electrodes** which are sequentially formed on **trench** grooves formed by etching base and emitter layers
Patent Assignee: FUJI ELECTRIC CO LTD (FJIE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001320049	A	20011116	JP 2000135717	A	20000509	200216	B

Priority Applications (No Type Date): JP 2000135717 A 20000509
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001320049	A		11	H01L-029/78	

Abstract (Basic): JP 2001320049 A
Abstract (Basic):
NOVELTY - The buffer layers (2a,2b), p-type base layers (3a,3b), n-type emitter layers (4a,4b) and **electrodes** (6a,6b) are sequentially formed on either sides of a n-type drift layer (1). **Trench** grooves (8a,8b) are formed on the buffer layers by sequentially etching the base and the emitter **layers**. The gate **insulating films** (7a,7b) and gate **electrodes** (5a,5b) are sequentially formed on the **trench** grooves.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **semiconductor device** manufacturing method.
USE - **Semiconductor device** e.g. bidirectional insulated **gate bipolar transistor** (**IGBT**) for electric power converter.
ADVANTAGE - Stabilizes ON state voltage and reduces size and manufacturing cost as the turn-off losses are reduced.
DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the **semiconductor device**. (Drawing includes non-English language text).
n-type drift layer (1)
Buffer layers (2a,2b)
p-type base layers (3a,3b)
n-type emitter layers (4a,4b)
Gate **electrodes** (5a,5b)
Electrodes (6a,6b)
Gate **insulating films** (7a,7b)
Trench grooves (8a,8b)
pp; 11 DwgNo 1/17

43/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014077862
WPI Acc No: 2001-562076/200163
XRPX Acc No: N01-418185
Semiconductor device e.g. insulated **gate bipolar transistor** has **trench** having linear and arc-shaped sections which are connected continuously without break so that current is passed between main and back surfaces of substrate
Patent Assignee: NIPPONDENSO CO LTD (NPDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001217419	A	20010810	JP 200032617	A	20000203	200163	B

Priority Applications (No Type Date): JP 200032617 A 20000203
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001217419	A		7	H01L-029/78	

Abstract (Basic): JP 2001217419 A
Abstract (Basic):
NOVELTY - **Trench** (6) is formed on the main surface of a **semiconductor** substrate. A gate **insulating film** (7) is formed on inner wall surface of **trench** and gate **electrode** (8) on surface of the film. The **trench** has linear portions (6a) and arc-shaped portions (6b) which are connected continuously without break, so that the current is passed between main surface and back surface of the substrate.
USE - **Semiconductor device** with **trench** gate e.g. metal oxide **semiconductor** field effect transistor (MOSFET), insulated **gate bipolar transistor** (**IGBT**).
ADVANTAGE - Enhances gate insulation pressure resistance as the **trench** does not have any break and is formed continuously.
DESCRIPTION OF DRAWING(S) - The figure shows the layout of insulated **gate bipolar transistor**. (Drawing includes non-English language text).
Trench (6)
Linear portion (6a)
Arc shaped portion (6b)
Gate **insulating film** (7)
Gate **electrode** (8)
pp; 7 DwgNo 1/8

43/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013858503
WPI Acc No: 2001-342716/200136
Related WPI Acc No: 2000-349416
XRAM Acc No: C01-105967
XRPX Acc No: N01-248201
Semiconductor device in silicon substrate of first conductivity has **trench**, first and overlaying **insulating layers**, regions of polysilicon and second conductivity type, impurities region of first **conductivity** and **conductive layer**
Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: LIZOTTE S C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6229194	B1	20010508	US 98114546	A	19980713	200136 B
			US 2000481045	A	20000111	

Priority Applications (No Type Date): US 98114546 A 19980713; US 2000481045 A 20000111
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6229194	B1		17	H01L-029/00	Div ex application US 98114546 Div ex patent US 6054365

Abstract (Basic): US 6229194 B1
Abstract (Basic):
NOVELTY - A **semiconductor device** in silicon substrate of first conductivity type comprises **trench** separating and surrounding each cell in substrate; first **insulating layer** on lower portion of **trench** walls; regions of polysilicon and second conductivity type; impurities region of first **conductivity** type; overlaying **insulation layer** having openings; and **conductive layer** having interconnecting contacts.
DETAILED DESCRIPTION - A **semiconductor device** in silicon substrate of first conductivity type consists of **trench**, first **insulating layer** (50), region of polysilicon, region of second conductivity type, impurities region of first **conductivity** type, overlaying **insulation layer** (60), and **conductive layer**. The **trench** separates and surrounds each of at least two cells in the substrate and extends from the top to the bottom surface of the substrate. The first **insulating layer** is formed only on a lower portion of the **trench** walls and arranged so that an upper portion of the **trench** walls remains free. The region of polysilicon is formed in the **trench** and extends from top to bottom surface of the substrate between the **insulating** material **layer**. The region of second conductivity type is formed on the top surface of silicon substrate. The impurities region of first conductivity type is formed

on top surface of the substrate and is spaced from and surrounds the region of second conductivity type. The overlaying **insulation layer** on top surface of the substrate has opening(s) to the region of first conductivity type in one of the cells and to the region of second conductivity type adjoining one of the cells. The **conductive layer** comprises interconnecting contact(s), which connect the regions of first conductivity type of the respective cell and second conductivity type of the adjoining cell.

USE - Used as **semiconductor device** e.g. photovoltaic generator, metal oxide **semiconductor** field effect transistors or isolated **gate bipolar transistors**.

ADVANTAGE - The device is formed using simple and inexpensive starting wafer so reducing its cost. The more expensive processing steps, e.g. **trench** formation and **trench** filling with dielectric and polysilicon, can be formed towards the end of the process.

DESCRIPTION OF DRAWING(S) - The figures show the device.

First **insulating layer** (50)

Second **insulating layer** (51)

Overlaying **insulation layer** (60)

Passivation layer (80)

pp; 17 DwgNo 5, 6/11

43/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013653027
WPI Acc No: 2001-137239/200114
Related WPI Acc No: 2001-089738
XRAM Acc No: C01-040173
XRPX Acc No: N01-099929
Formation of an isolation structure of, e.g., metal-oxide **semiconductor** field-effect transistor, involves forming a refill material within the **trench** region to cover the respective top corners of the active regions
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: JOYNER K A; LOEWENSTEIN L M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6180491	B1	20010130	US 9632734	A	19961213	200114 B
			US 97987226	A	19971209	
			US 99335096	A	19990617	

Priority Applications (No Type Date): US 9632734 P 19961213; US 97987226 A 19971209; US 99335096 A 19990617
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6180491	B1		6	H01L-021/76	Provisional application US 9632734 Div ex application US 97987226 Div ex patent US 6114741

Abstract (Basic): US 6180491 B1
Abstract (Basic):
NOVELTY - An isolation structure is formed by providing a diffusion barrier over the pad **dielectric layer** on a substrate, forming a **trench** between the two regions of the substrate, removing a portion of diffusion barrier, covering the respective top corners of the active regions, removing the diffusion barrier and the pad **layer**, and forming gate **conductor** over a gate **dielectric layer**.
DETAILED DESCRIPTION - Formation of an isolation structure comprises forming a diffusion barrier over a pad **dielectric layer** on a substrate (10); forming a **trench** region between the first and second active region of the substrate; removing a portion of the diffusion barrier layer above the respective top corners (30, 32) of the two active regions (12, 14); forming a refill (22) material within the **trench** region to cover a portion of the corners; removing the diffusion barrier **layer** and the pad **dielectric layer**; forming gate **dielectric layer** on the respective upper surface of the two active regions; and forming a gate **conductor layer** (26) on an upper surface of the gate **dielectric layer** (24).
USE - The method is used for forming an isolation structure of a **semiconductor devices** such as metal-oxide

semiconductor field-effect transistor. It may be used when shallow **trench** isolation techniques are used in bulk silicon substrates and when mesa isolation techniques are used in silicon-on-insulator substrates.

ADVANTAGE - The method prevents the formation of parasitic transistor having a threshold voltage that less than the threshold voltage of the main transistor device. It reduces or eliminates off-state leakage currents and increases gate oxide integrity thus improving overall system reliability in the fabrication of metal-oxide **semiconductor** field effect transistor, bicomplementary metal-oxide **semiconductor** circuits, isolated **gate bipolar transistor**, and any device having sharp corner or edge. It decreases heat dissipation and power consumption.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional diagrams of an isolation structure.

Substrate (10)
Active regions (12, 14)
Refill (22)
Dielectric layer (24)
Conductor layer (26)
Corners (30, 32)
pp; 6 DwgNo 1E/1

43/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013603659
WPI Acc No: 2001-087866/200110
XRPX Acc No: N02-166562
Trench insulated **gate bipolar transistor** for power electronic device, has channel stop region with a portion overlapping emitter region, so that **conductive** channel in base region does not directly contact emitter region
Patent Assignee: FAIRCHILD KOREA SEMICONDUCTOR CO LTD (FAIH); SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: KIM T H; LEE G H; KIM T; LEE K
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2000015138	A	20000315	KR 9834881	A	19980827	200110	B
US 6262470	B1	20010717	US 99369487	A	19990805	200228	
KR 275756	B	20001215	KR 9834881	A	19980827	200175	

Priority Applications (No Type Date): KR 9834881 A 19980827
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2000015138	A			H01L-029/74	
US 6262470	B1		8	H01L-027/082	
KR 275756	B			H01L-029/74	Previous Publ. patent KR 2000015138

Abstract (Basic): US 6262470 B1
Abstract (Basic):
NOVELTY - Emitter regions (150,150P) are formed overlying the base region (130) formed on a drift region (120) formed on a **semiconductor** substrate (100). Channel stop region (140) is interposed in between base and emitter regions. Channel stop region has a portion overlapping the emitter region, so that **conductive** channel formed in the base region does not directly contact the emitter region.

DETAILED DESCRIPTION - Gate **insulative layer** (160) is formed on the inner wall of **trench** formed contacting the drift region. Gate **electrode** is formed on the gate **insulative layer**. Channel stop region has another portion not overlapping the emitter region.

USE - For power electronic device e.g. invertor, converter and switching power supply.

ADVANTAGE - Suppresses latch-up phenomenon by decreasing amount of voltage drop due to hole current by doping the channel stop region with high concentration P-type impurities.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional view of **trench** insulated **gate bipolar transistor**.

Semiconductor substrate (100)
Drift region (120)
Base region (130)

Channel stop region (140)
Emitter regions (150,150P)
Gate **insulative layer** (160)
pp; 8 DwgNo 4/5

43/3,AB/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013521844
WPI Acc No: 2001-006050/200101
Related WPI Acc No: 1999-034214; 2000-564335
XRAM Acc No: C01-001255
XRPX Acc No: N01-004280
Fabrication of bipolar device circuit involves forming **dielectric layer** on surface of substrate with interconnected **semiconductor devices**
Patent Assignee: ADAMIC F W (ADAM-I)
Inventor: ADAMIC F W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6124179	A	20000926	US 96711376	A	19960905	200101 B
			US 9816745	A	19980130	

Priority Applications (No Type Date): US 96711376 A 19960905; US 9816745 A 19980130
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6124179	A		29	H01L-021/764	Cont of application US 96711376 Cont of patent US 5841197

Abstract (Basic): US 6124179 A
Abstract (Basic):
NOVELTY - A bipolar device circuit is fabricated by forming a **dielectric layer** on a surface of substrate having interconnected **semiconductor devices** and bonding a support substrate to the substrate first surface to form composite structure.
DETAILED DESCRIPTION - A bipolar device circuit (200) is fabricated on a substrate (202) by doping active regions of a device on substrate's first side (222), forming insulated interconnects interconnecting the active regions, forming a **dielectric layer** (206) on the first side overlying the interconnects, bonding a support (224) to the first side overlying the **dielectric layer** to form a composite structure, removing a portion of the substrate opposite the substrate's first side so that only active regions remain, doping second-side regions of the device into the substrate's second side (244), and forming a second-side **conductor**.
USE - For fabricating a bipolar device circuit on a substrate.
ADVANTAGE - The invention reduces leadout resistance by incorporating a **conductive layer** in close proximity to an active collector or drain region. The device has an improved high frequency performance resulting from the reduced base sidewall capacitance and collector leadout resistance.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the invention.
Bipolar device circuit (200)

Substrate (202)
Dielectric layer (206)
NPN transistor (212)
PNP transistor (214)
Bond layer (219)
Interface metal layer (221)
Substrate first side (222)
Support (224)
Substrate second side (244)
Emitter (281)
Isolation **trenches** (292)
pp; 29 DwgNo 2E/10

43/3,AB/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013457692
WPI Acc No: 2000-629635/200061
XRAM Acc No: C00-188796
XRPX Acc No: N00-466626
Power **trench** MOS-gated device has a heavily doped **semiconductor** substrate with a doped **conductive** upper **layer** containing a **trench** gate
Patent Assignee: INTERSIL CORP (INTE-N); KOCON C B (KOCO-I)
Inventor: KOCON C; KOCON C B
Number of Countries: 028 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1041640	A2	20001004	EP 2000104705	A	20000303	200061 B
JP 2000299464	A	20001024	JP 200091296	A	20000329	200104
US 20010001494	A1	20010524	US 99283536	A	19990401	200130
KR 2000071468	A	20001125	KR 200014626	A	20000322	200131

Priority Applications (No Type Date): US 99283536 A 19990401
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1041640	A2	E	14	H01L-029/78	
JP 2000299464	A		10	H01L-029/78	
US 20010001494	A1			H01L-029/76	
KR 2000071468	A			H01L-021/336	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

Abstract (Basic): EP 1041640 A2
Abstract (Basic):
NOVELTY - Power **trench** MOS-gated device (200) includes a heavily doped **semiconductor** substrate (201), a doped upper layer (202) of a first **conduction** type on the substrate and a **trench** gate in the upper **layer** by an **insulating layer**.
DETAILED DESCRIPTION - The **trench** gate comprises a **conductive** material separated from the upper **layer** by an insulating **layer**, an enhanced **conductivity** drain region underlying the **trench** gate in the upper layer. A heavily doped source region of first **conduction** type and a heavily doped body region of opposite **conduction** type are at an upper surface of the upper layer. A deep well region of the second **conduction** type is placed in the upper layer underlying the source and body regions. The deep well region extends below the **trench** gate and abuts the enhanced conductivity drain region, in which the enhanced region is more heavily doped than the doped upper layer.
USE - For power MOSFET, insulated **gate bipolar transistor** and MOS controlled thyristor.
DESCRIPTION OF DRAWING(S) - The drawing shows a power **trench** MOS-gated transistor.

device (200)
semiconductor substrate (201)
doped upper layer (202)
pp; 14 DwgNo 16/21

43/3,AB/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013441520
WPI Acc No: 2000-613463/200059
XRAM Acc No: C00-183743
XRPX Acc No: N00-454513
High density metal oxide **semiconductor** gated **device** e.g., power metal oxide **semiconductor** field effect transistor includes a shallow body region underlying a source region contact area
Patent Assignee: INTERSIL CORP (INTE-N)
Inventor: KOCON C; ZENG J; KOCON C B
Number of Countries: 028 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1041638	A1	20001004	EP 2000106130	A	20000321	200059	B
JP 2000307115	A	20001102	JP 200097006	A	20000331	200061	
US 6188105	B1	20010213	US 99283531	A	19990401	200111	
KR 2000076870	A	20001226	KR 200013128	A	20000315	200134	

Priority Applications (No Type Date): US 99283531 A 19990401
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1041638	A1	E	21	H01L-029/10	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
JP 2000307115	A		16	H01L-029/78	
US 6188105	B1			H01L-029/76	
KR 2000076870	A			H01L-029/78	

Abstract (Basic): EP 1041638 A1
Abstract (Basic):
NOVELTY - High density metal oxide **semiconductor** (MOS)-gated device includes a shallow body region (211) underlying a source region (201) contact area.
DETAILED DESCRIPTION - High density metal oxide **semiconductor** (MOS)-gated device includes a **semiconductor** substrate (101) and a doped upper **layer** of a first **conduction** type on the substrate. The upper layer comprises a heavily doped source region (201) of the first **conduction** type and a doped well region (103) of a second and opposite **conduction** type at an upper surface. The upper surface comprises a contact area for the source region and a recessed portion that comprises a contact area for a heavily doped deep body region of the second **conduction** type in the upper layer. The deep body region lies under the recessed portion. A **trench** gate is disposed in the upper layer. The **trench** gate comprises a **conductive** material (205) separated from the upper **layer** by an **insulating layer**. A shallow body region (211) lies under the source region contact area. The device is selected from a power metal oxide **semiconductor** field effect transistor (MOSFET), an insulated **gate bipolar transistor** and a MOS-controlled thyristor.

INDEPENDENT CLAIMS are also included for methods for forming a high density MOS-gated device.

USE - None given.

ADVANTAGE - The metal oxide **semiconductor** (MOS) **device** has reduced device size and improved efficiency and power handling capability.

DESCRIPTION OF DRAWING(S) - The diagram shows a cross-section of the MOS-gated device.

Substrate (101)
Epitaxial layer (102)
P-well (103)
N+ source (201)
Polysilicon (205)
Inter-level dielectric (207)
Shallow body region (211)
Metal layer (212)
pp; 21 DwgNo 31/31

43/3,AB/15 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013327949
WPI Acc No: 2000-499888/200045
XRPX Acc No: N00-370515
Insulated **gate bipolar transistor** with improved on-state voltage - has multiple layers in region of pn-junction to increase charge carriers directly in front of pn-junction
Patent Assignee: SIEMENS AG (SIEI)
Inventor: MILLER G; STRACK H; TIHANYI J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 19904103	A1	20000810	DE 1004103	A	19990202	200045	B

Priority Applications (No Type Date): DE 1004103 A 19990202
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19904103	A1		7	H01L-029/739	

Abstract (Basic): DE 19904103 A
The **IGBT** includes an **semiconductor** (1) of a n-type. In the region of the first surface of the **semiconductor**, a p-type **trench** zone (3) is provided. In the **trench** zone (3), highly doped n-type drain and source zones are provided. A gate **electrode** is provided over the **trench** zone in the region between the source zone and the drain zone, and is separated from the first surface by an **insulating layer** (6).
An emitter layer (2) of the p- type is provided in the region of the second surface. Multiple layers (8) consisting at least of one n-type layer (9) and one p-type layer (10) are embedded in the **semiconductor**, bordering on the **trench** zone.
USE - **IGBT**.
ADVANTAGE - Reduced on-state losses, and simple manufacture.
Dwg.1/4

43/3,AB/16 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013295066
WPI Acc No: 2000-467001/200041
XRPX Acc No: N00-348551
Power metal oxide **semiconductor** field effect transistor (MOSFET) - has **trenches** provided in **semiconductor** body and extending through the trough zone between drain zone and source zone
Patent Assignee: SIEMENS AG (SIEI)
Inventor: TIHANYI J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 19900648	A1	20000720	DE 1000648	A	19990111	200041	B

Priority Applications (No Type Date): DE 1000648 A 19990111
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19900648	A1		5	H01L-029/78	

Abstract (Basic): DE 19900648 A

A power MOSFET includes a **semiconductor** body (1) of a first conductivity type and is provided with a drain zone; a trough zone (2) is provided in the **semiconductor** body and has a conductivity type opposite to the first type. A source zone (4) is provided in the trough zone and is of the first conductivity type.

An **insulating layer** (5) covers the surface of the trough zone at least between the drain zone and the source zone, and a gate **electrode** is provided on the **insulating layer** between the drain zone and the source zone. **Trenches** (7) are made in the **semiconductor** body and extend through the trough zone, parallel to the direction between the drain zone and the source zone. The walls of the **trenches** are provided with an **insulating layer** (15) and the **trenches** are filled out in the remaining parts with a **conducting** material (8), the latter specifically being highly doped polycrystalline silicon having charge-carriers of the first conductivity type.

USE - **Bipolar transistor** with insulated gate (**IGBT**).

ADVANTAGE - Despite relatively small surface area, has large channel zone elongation.

Dwg.1-3/5

43/3,AB/17 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011594654
WPI Acc No: 1998-011782/199802
XRPX Acc No: N98-009343
Semiconductor trench device for insulated **gate** **bipolar transistor** - has electrically **conductive** region that extends to depth of bottom of **trench** and composed of material having conductivity type opposite to that region immediately underlying **trench**
Patent Assignee: PLESSEY SEMICONDUCTORS LTD (PLES)
Inventor: AMARATUNGA G A J; UDREA F
Number of Countries: 019 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2314206	A	19971217	GB 9612397	A	19960613	199802	B
EP 813250	A2	19971217	EP 97304045	A	19970609	199804	
JP 10070271	A	19980310	JP 97168083	A	19970610	199820	

Priority Applications (No Type Date): GB 9612397 A 19960613
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2314206	A		21	H01L-029/739	
EP 813250	A2	E	16	H01L-029/06	
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
JP 10070271	A		7	H01L-029/78	

Abstract (Basic): GB 2314206 A

The **trench** device includes an active region (8) having one or more **trenches** (19,20) extending from its first surface with at least one p-n junction associated across whose current flow is controllable by a gate **electrode** region disposed at a side wall of the **trench**. An electrically **conductive** region (12,13) encircles the active region. The electrically **conductive** region extends to the depth of the bottom of the **trench** and is composed of a **semiconductor** material having a conductivity type opposite to that of the **semiconductor** region immediately underlying the **trench**.

The electrically **conductive** region is an electrically floating region that encircles all of the **trenches** forming part of a common **trench** around its perimeter. The electrically floating region extends from the surface of the device to a depth which is the same as the **trench**. The electrically floating region is in part a local region of the required conductivity type formed at the bottom of a further **trench**.

ADVANTAGE - Capable of operating at high power and voltage levels. Improved breakdown at edge of device that improves irs performance.

Dwg.4/14

43/3,AB/18 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010855462
WPI Acc No: 1996-352415/199635
XRPX Acc No: N96-297284
Semiconductor device e.g. vertical insulated **gate** **bipolar transistor** with **trench** gate structure - has **trench** which penetrates n-type source, p-type base and n-type low concentration drain piled together in which upper part of **trench** is covered with source metal **electrode**
Patent Assignee: TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8167716	A	19960625	JP 94333001	A	19941214	199635	B
JP 3288878	B2	20020604	JP 94333001	A	19941214	200240	

Priority Applications (No Type Date): JP 94333001 A 19941214
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8167716	A		9	H01L-029/78	
JP 3288878	B2		8	H01L-029/78	Previous Publ. patent JP 8167716

Abstract (Basic): JP 8167716 A

The device includes an n-type low concentration drain (2) formed on a **semiconductor** substrate (20). A p-type base (3) is formed on the surface of the drain. An n-type source (4) is formed on the p-type base. Several **trenches** (5) are formed penetrating from the source to the base and to the drain. The inner wall surface of each **trench** is covered with a gate **insulating film** (6).

A gate **electrode** (7) is implanted in each **trench**. The upper part of the **trench** is covered with an **insulating film** (15). A gate metal **electrode** (11) is placed on the **insulating film** of the **trench** nearest the edge and is electrically connected to the gate **electrode**. The other **trenches** are covered with a source metal **electrode** (10).

ADVANTAGE - Increase resistance to small number of carrier supplied from anode **electrode** and increases storing effect of carrier near base. Raises deg. modulation effect of **conduction** and decreases ON state voltage.

Dwg.1/12

43/3,AB/19 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010684375
WPI Acc No: 1996-181331/199619
XRAM Acc No: C96-057275
XRPX Acc No: N96-152368

Trench-gate field-effect **semiconductor device** (MOSFET or **IGBT**) - has high **conductivity** buried **layer** contact embedded in the base/substrate region improving contact between source region and **electrode**

Patent Assignee: SIEMENS AG (SIEI)
Inventor: TIHANYI J
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 706223	A1	19960410	EP 95114820	A	19950920	199619	B
DE 4435458	A1	19960411	DE 4435458	A	19941004	199620	
JP 8213598	A	19960820	JP 95278403	A	19951002	199643	
DE 4435458	C2	19980702	DE 4435458	A	19941004	199830	
US 5869864	A	19990209	US 95539175	A	19951004	199913	
			US 97834311	A	19970415		

Priority Applications (No Type Date): DE 4435458 A 19941004
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 706223	A1	G	5	H01L-029/10	
Designated States (Regional): DE FR IT					
DE 4435458	A1		4	H01L-029/78	
JP 8213598	A		4	H01L-029/78	
US 5869864	A			H01L-029/76	CIP of application US 95539175
DE 4435458	C2			H01L-029/78	

Abstract (Basic): EP 706223 A

The source (3) is embedded in the base zone (2) which is within the inner-zone (1). Above the source (3) lies the gate region (6) which is encapsulated in **insulating layers** (7,5). On the source side a contact window through the **insulating layers** (5,7) connects the **electrode** (8) to the source and base region (2,3). The other side of the device is connected to another **electrode** (9) via the anode zone (4). To improve the contact between the **electrode** (8) and the base region (2), a buried layer (10), connected to the **electrode** (8), with higher conductivity (e.g., highly doped polysilicon or metal) than the base region (2), is built laterally jutting out over the source region (3). This affects the device's operating voltage.

ADVANTAGE - Elimination of potentially destructive, parasitic **bipolar transistor** between source, base and inner zones.

Dwg.1/2

43/3,AB/20 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010091411
WPI Acc No: 1994-359124/199445
XRPX Acc No: N94-281364
MOS **semiconductor device** preventing erroneous operation caused by parasitic **bipolar transistor** - has structured **insulation layer** supporting gate **electrode** with source zone on top isolated by another **insulation layer**
Patent Assignee: SIEMENS AG (SIEI)
Inventor: STRACK H
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4315723	A1	19941117	DE 4315723	A	19930511	199445	B
JP 7015008	A	19950117	JP 94119552	A	19940509	199512	
US 5396088	A	19950307	US 94240138	A	19940510	199515	
DE 4315723	C2	19951005	DE 4315723	A	19930511	199544	

Priority Applications (No Type Date): DE 4315723 A 19930511
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4315723	A1		4	H01L-029/784	
JP 7015008	A		3	H01L-029/78	
US 5396088	A		4	H01L-029/78	
DE 4315723	C2		4	H01L-029/78	

Abstract (Basic): DE 4315723 A

The source areas (14) of an MOS **semiconductor device** are arranged upon the side of the gaze **electrode** (4). The upper surface of the source regions are contacted by source **electrode** (6). The base region (5) borders the side of the source region and gaze **electrode** and contacts drain region (1).

The new structure prevents the flow of minority charges from drain region to the source **electrode** via the source region. Instead these charges flow directly through the base region bordering the gate **electrode**, towards the source **electrode**.

The same principle of construction can be used for **trench** -MOS, U-MOS or V-MOS transistors.

ADVANTAGE - Prevents switching on of parasitic **bipolar transistor** and thus, avoids effect known as ''second breakdown''.

Dwg.1/2

Abstract (Equivalent): DE 4315723 C

The MOSFET has a lightly doped n-type drain region (1) with a surface (2) on the source side covered by a structured **insulating layer** (3) under the gate **electrode** (4). More insulation (13) separates the gate from a source region (14) against which a lightly-doped p-type base region (5) abuts laterally.

The base region overlaps the gate and abuts against the drainer region. The source **electrode** (6) contacts the source region on the side remote from the gate. A more heavily doped n-type region (9)

(for an **IGBT**, a p-type region) covers the opposite side of the **semiconductor** body.

ADVANTAGE - **Conduction** through the parasitic bipolar structure is prevented reliably, with limitation of the **IGBT** current gain to less than unity in all circumstances.

Dwg.1/2

Abstract (Equivalent): US 5396088 A

The MOS component on a horizontally oriented **semiconductor** body, comprises at least one drain zone in the horizontally oriented **semiconductor** body, at least one base zone on the horizontally oriented **semiconductor** body and at least one source zone. At least one gate **electrode** is disposed over the drain zone and electrically insulated from the source zone and the drain zone, the source zone being vertically stacked on and over the gate **electrode**.

A portion of the base zone extends to laterally adjoin the source zone next to the gate **electrode** and is electrically insulated from the gate **electrode**. A source **electrode** is electrically contacted with the source zone on a surface facing away from the gate **electrode**. Each of the drain zone and the gate **electrode** have respective planar surfaces, with the planar surface of the base zone overlaps the planar surface of the gate **electrode**.

ADVANTAGE - Reliably prevents activation of parasitic bipolar structure.

Dwg.1/2

43/3,AB/21 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06642705
TRENCH INSULATED **GATE BIPOLAR TRANSISTOR**

PUB. NO.: 2000-228519 [JP 2000228519 A]
PUBLISHED: August 15, 2000 (20000815)
INVENTOR(s): YOSHIKAWA ISAO
APPLICANT(s): FUJI ELECTRIC CO LTD
APPL. NO.: 11-028392 [JP 9928392]
FILED: February 05, 1999 (19990205)

ABSTRACT

PROBLEM TO BE SOLVED: To improve saturation voltage to turn-off loss trade-off characteristics by constituting that a first **conductivity** drift **layer** appears on the main surface of a **semiconductor** substrate in the region in which the second conductivity well region is not formed.

SOLUTION: **Trenches** 7 are formed with certain intervals on the main surface of one side of an n-type (a first **conductive** type) drift **layer** 1, a p-type (a second **conductive** type) well region 2 is selectively formed parallel to and in contact with this, and an (n) source region 3 is formed on a surface layer thereof. A part of the surface of the (n) source region 3 and the p-type (the second **conductive** type) well region 2 are removed and an **insulating film** 8 covers the main surface. Then, in the region in which the p-type (the second **conductive** type) well region 2 is not formed, the n-type (the first **conductive** type) drift **layer** 1 is allowed to reach the surface. In other words, a structure in which a part of the main surface is not covered with the p-type (the second **conductive** type) well region 2 is formed. The width of the n-type (the first **conductive** type) drift **layer** 1 should be about 80 μm.

43/3,AB/22 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

04446102
TRENCH INSULATED **GATE** **BIPOLAR TRANSISTOR** AND ITS PRODUCTION

PUB. NO.: 06-090002 [JP 6090002 A]
PUBLISHED: March 29, 1994 (19940329)
INVENTOR(s): AKIYAMA HAJIME
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-240666 [JP 92240666]
FILED: September 09, 1992 (19920909)
JOURNAL: Section: E, Section No. 1572, Vol. 18, No. 350, Pg. 30, June 30, 1994 (19940630)

ABSTRACT

PURPOSE: To provide a T-**IGBT** and its production by which on-state voltage can be decreased for refining.

CONSTITUTION: An n(sup -) epitaxial layer 3 is formed on a p(sup +) collector layer 1 and further a p well area 4 is formed thereon. An n(sup +) emitter area 5 is formed on the surface of the area 4. A groove 7 is prepared in a manner to extend over from the surface of the area 5 to the layer 3 and the internal surface of the groove 7 is provided with a gate **electrode** 3 with a gate **insulating film** 6 interposed. The surfaces of the areas 5 and 4 is provided with an emitter **electrode** 9 and the rear surface of the layer 1 is provided with a collector **electrode** 10. A p-type impurity layer 19 is formed just beneath the bottom face of the groove 7. The sum of the width W(sub p2) of the layer 19 and the width W(sub p1) of the surface of the area 4 is 50 to 70% of the unit cell width w(sub s/2).

47/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014403916
WPI Acc No: 2002-224619/200228
XRPX Acc No: N02-172084
Non-volatile **semiconductor** memory **device**, with partial-**trench**-isolation insulating film not reaching buried oxide layer in memory cell transistor
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: KUNIKIYO T; MAEDA S; MATSUMOTO T
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6314021	B1	20011106	US 2000715141	A	20001120	200228	B
DE 10064200	A1	20011220	DE 1064200	A	20001222	200228	
JP 2001351995	A	20011221	JP 2000171793	A	20000608	200228	
KR 2001110976	A	20011215	KR 20011159	A	20010109	200238	

Priority Applications (No Type Date): JP 2000171793 A 20000608
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6314021	B1		45	G11C-007/00	
DE 10064200	A1			H01L-027/115	
JP 2001351995	A		26	H01L-021/8247	
KR 2001110976	A			H01L-027/115	

Abstract (Basic): US 6314021 B1
Abstract (Basic):
NOVELTY - In a memory cell transistor of a flash memory, a silicon substrate (2), buried oxide layer (BOX) (3), and silicon layer (4) form a silicon on insulator (SOI) substrate (1) in that order. In the upper surface of the silicon layer a partial-**trench**-isolation insulating film (5) is formed that does not reach the upper surface of the BOX layer.

DETAILED DESCRIPTION - In an element formation **region** defined by the **partial-trench**-isolation insulating film, inside the upper surface of the silicon layer, are a source and drain region paired with a body region (70) in between them. On the upper surface of the silicon layer, where the body region is formed, a **multi layer** structure, in which a gate oxide film (6), a floating gate (7), an insulating film (8) and a control gate (9) are layered in this order, constituting a gate electrode structure.

ADVANTAGE - The partial-**trench**-isolation insulating film is used instead of the conventional full-isolation insulating film, to externally fix a potential of the body region through the silicon layer between the upper surface of BOX layer and partial-isolation insulating film. Therefore it is possible to avoid a malfunction caused by accumulation of the positive holes in the body region and enhance a breakdown voltage between the source and drain. As a result, a memory cell transistor which can perform write and read operations of data with a high voltage, is obtained.

It is also possible to enhance the source-drain breakdown voltage.

DESCRIPTION OF DRAWING(S) - A cross-section drawing of the structure of a memory cell transistor in a non-volatile **semiconductor** memory **device** is shown. Partial-**trench** -isolation insulating film (5)silicon substrate (2)buried oxide layer (3)silicon layer (4)SOI substrate (1)body region (70)gate oxide film (6)floating gate (7)insulating film (8)control gate (9)

pp; 45 DwgNo 1/50

47/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014374655
WPI Acc No: 2002-195358/200225
XRAM Acc No: C02-060295
XRPX Acc No: N02-148437
Microelectronic structure, e.g. field effect transistors, has at least one shallow **trench** isolation structure of first conductivity type that is **partially** isolated from **region** of second conductivity type
Patent Assignee: INTEL CORP (ITLC)
Inventor: CHAU R S; MCFADDEN R S; MORROW P; MURTHY A S
Number of Countries: 094 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200150535	A2	20010712	WO 2000US42279	A	20001127	200225	B
AU 200143057	A	20010716	AU 200143057	A	20001127	200225	

Priority Applications (No Type Date): US 99474836 A 19991230
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200150535	A2	E	23	H01L-029/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

AU 200143057	A			H01L-029/00	Based on patent WO 200150535

Abstract (Basic): WO 200150535 A2
Abstract (Basic):
NOVELTY - A microelectronic structure has a substrate (201) comprising at least one shallow **trench** isolation structure (210) of first conductivity type.
The substrate has at least one recess having a bottom and side surfaces. A gate dielectric layer is disposed on the bottom of the recess. A gate electrode of second conductivity type is formed superadjacent the gate dielectric layer
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of forming a shallow **trench** isolation structures comprising:
(a) masking a portion of **semiconductor** surface;
(b) forming a recess in the surface adjacent to the masked portion;
(c) implanting ions to a bottom surface of the recess; and
(d) forming an undoped silicon layer within the recess.
USE - As microelectronic structures for **semiconductor devices**.
ADVANTAGE - The device has reduced junction capacitance, and charge leakage pathways between the STI and the substrate. The STI are provided with shielding from carriers generated by alpha particle

strikes.

DESCRIPTION OF DRAWING(S) - The figure is a schematic cross-section of the shallow **trench** isolation structure of a metal oxide field effect transistor.

Substrate (201)
Gate electrode (202)
Barrier layer (204)
Spacers (206)
Gate dielectric layer (208)
Shallow **trench** isolation structure (210)
Recess (212)
pp; 23 DwgNo 2/7

47/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011557963
WPI Acc No: 1997-534444/199749
XRAM Acc No: C97-170691
XRPX Acc No: N97-445011
High pressure metal oxide **semiconductor device** - replacing conventional implanted heavily doped source-drain structure by **trenched** source-drain
Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)
Inventor: UEN R; WEN J
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 313674	A	19970821	TW 96111563	A	19960921	199749	B
US 5696009	A	19971209	US 96749794	A	19961115	199804	
US 5910666	A	19990608	US 96749794	A	19961115	199930	
			US 97928627	A	19970912		

Priority Applications (No Type Date): TW 96111563 A 19960921
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 313674	A		18	H01L-021/18	
US 5696009	A		10	H01L-021/8234	
US 5910666	A			H01L-029/76	Div ex application US 96749794 Div ex patent US 5696009

Abstract (Basic): TW 313674 A
Manufacture of high pressure metal oxide **semiconductor device** comprises: (1) on one first-type substrate in sequence forming one pad oxide and one silicon nitride; (2) forming one photoresist, by photolithography process patterning the photoresist and performing second electricity implantation, in the first-type substrate forming multiple well **regions**; (3) removing **partial** silicon nitride, with the silicon nitride as mask implanting one second electricity ion into the first-type substrate;(4) forming one isolation, in the same time under the isolation **layer** forming **multiple** drift region; (5) removing the silicon nitride and the pad oxide; (6) on predetermined position forming multiple **trenches**, in which those **trenches** penetrate the isolation and those drift region, but not those well regions; (7) forming one first conductive layer, filling those **trenches**; (8) patterning the first conductive layer, forming source/drain region;(9) in sequence forming one gate oxide and one second conductive layer;(10) patterning the gate oxide and the second conductive layer, forming one gate.
Dwg.0/2
Abstract (Equivalent): US 5696009 A
Manufacture of high pressure metal oxide **semiconductor device** comprises: (1) on one first-type substrate in sequence forming one pad oxide and one silicon nitride; (2) forming one photoresist, by photolithography process patterning the photoresist and

performing second electricity implantation, in the first-type substrate forming multiple well **regions**; (3) removing **partial** silicon nitride, with the silicon nitride as mask implanting one second electricity ion into the first-type substrate;(4) forming one isolation, in the same time under the isolation **layer** forming **multiple** drift region; (5) removing the silicon nitride and the pad oxide; (6) on predetermined position forming multiple **trenches**, in which those **trenches** penetrate the isolation and those drift region, but not those well regions; (7) forming one first conductive layer, filling those **trenches**; (8) patterning the first conductive layer, forming source/drain region;(9) in sequence forming one gate oxide and one second conductive layer;(10) patterning the gate oxide and the second conductive layer, forming one gate.

Dwg.0/2

47/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008569155
WPI Acc No: 1991-073190/199110
XRPX Acc No: N91-056631

Laser diode opto-electronic integrated circuit - has body defining laser diode with **multiple** quantum well active **layer** sandwiched between two cladding layers

Patent Assignee: EASTMAN KODAK CO (EAST)
Inventor: KAHEN K B; RAJESWARAN G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4995049	A	19910219	US 90529830	A	19900529	199110	B

Priority Applications (No Type Date): US 90529830 A 19900529

Abstract (Basic): US 4995049 A

The optoelectronic integrated circuit includes a body of a gp. III-V **semiconductor** material contg. a laser diode, a photodiode and/or field effect transistors. The body includes isolation **regions** extending **partially** therethrough which electrically isolate the laser diode from the photodiode and the field effect transistors. However, the isolation **regions** are **partially** transparent to light to allow some of the light generated by the laser diode to reach the photodiode. The laser diode photodiode and/or field effect transistors are electrically connected by conductive patterns on the body so as to form a desired circuit for controlling the laser diode.

The body defines a laser diode having a **multiple** quantum well active **layer** sandwiched between two cladding layers. The photodiode may also be formed by the active layer and cladding layers or can be formed by filling a **trench** in the body with a **semiconductor** material. The field effect transistor is formed in an insulated cap layer of undoped gallium arsenide on one of the cladding layers.

ADVANTAGE - Has single solid state structure and stable laser power output. (11pp Dwg.No.2/7

51/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013492370
WPI Acc No: 2000-664313/200064
XRAM Acc No: C00-201219
XRPX Acc No: N00-492270
Fabrication of an integrated circuit having **multiple** gate **dielectric layers** involves forming an oxidation resistant **layer** on the patterned **conductive layer**, and on the active regions
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: BAKER F K; CHEN W; PRINZ E J; WU K Y; YERIC G M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6133093	A	20001017	US 9815957	A	19980130	200064	B

Priority Applications (No Type Date): US 9815957 A 19980130
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6133093	A		10	H01L-021/336	

Abstract (Basic): US 6133093 A
Abstract (Basic):
NOVELTY - An integrated circuit is fabricated by forming an oxidation resistant **layer** on the patterned **conductive layer**, and on the second and third active regions.
DETAILED DESCRIPTION - Fabrication of an integrated circuit involves forming a field isolation region (12) within a **semiconductor** substrate (10). The field isolation region defines first, second and third active regions (14, 16, 18). A first gate **dielectric layer** (20) is formed on the first **dielectric layer**, and a patterned **conductive layer** is formed on the first gate **dielectric layer**. An oxidation resistant layer (24) is formed overlying the patterned **conductive layer**, and the second and third active regions. A first portion of the oxidation resistant layer overlying the second active region is removed. A second gate **dielectric layer** (30) is formed on the second active region. A second portion of the oxidation resistant layer overlying the third active region is removed. A third gate **dielectric layer** (36) overlying the third active region is formed. A **control** gate **electrode** (44) for a floating gate device (50) is formed overlying a portion of the patterned **conductive layer**.
USE - For fabricating an integrated circuit having **multiple** gate **dielectric layers**.
ADVANTAGE - The oxidation resistant layer protects portions of the **trench** isolation region when the gate **dielectric layers** of the respective high breakdown and low breakdown voltage transistors (52, 54) are formed. It minimizes etching and thinning or recessing of the field isolation region. It does not degrade device

isolation, thus improves the reliability of the integrated circuit.

DESCRIPTION OF DRAWING(S) - The figure illustrates the method of fabricating the integrated circuit.

Portion of the substrate (5)
Semiconductor substrate (10)
Field isolation region (12)
Active regions (14, 16, 18)
Gate **dielectric layers** (20, 30, 36)
Oxidation resistant layer (24)
Control gate **electrode** (44)
Floating gate device (50)
Transistors (52, 54)

54/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013327949
WPI Acc No: 2000-499888/200045
XRPX Acc No: N00-370515

Insulated **gate bipolar transistor** with improved on-state voltage - has **multiple layers** in region of pn-junction to increase charge carriers directly in front of pn-junction

Patent Assignee: SIEMENS AG (SIEI)
Inventor: MILLER G; STRACK H; TIHANYI J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 19904103	A1	20000810	DE 1004103	A	19990202	200045	B

Priority Applications (No Type Date): DE 1004103 A 19990202
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19904103	A1		7	H01L-029/739	

Abstract (Basic): DE 19904103 A

The **IGBT** includes an **semiconductor** (1) of a n-type. In the region of the first surface of the **semiconductor**, a p-type **trench** zone (3) is provided. In the **trench** zone (3), highly **doped** n-type drain and source zones are provided. A gate **electrode** is provided over the **trench** zone in the region between the source zone and the drain zone, and is separated from the first surface by an **insulating layer** (6).

An emitter layer (2) of the p- type is provided in the region of the second surface. **Multiple layers** (8) consisting at least of one n-type layer (9) and one p-type layer (10) are embedded in the **semiconductor**, bordering on the **trench** zone.

USE - **IGBT**.

ADVANTAGE - Reduced on-state losses, and simple manufacture.

Dwg.1/4

56/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007254049
WPI Acc No: 1987-251056/198736
XRAM Acc No: C87-106219
XRPX Acc No: N87-187872
MESFET structure - with gate in insulated **trench** joined to source-drain **electrodes** by high-**impurity semiconductor** layer
Patent Assignee: HITACHI LTD (HITA)
Inventor: GOTO S; IMAMURA Y; KOBAYASHI M; OKUHIRA H; TAKATANE S; USAGAWA T; TAKATANI S
Number of Countries: 003 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3706274	A	19870903	DE 3706274	A	19870226	198736	B
JP 62200771	A	19870904	JP 8641768	A	19860228	198741	
JP 62213173	A	19870919	JP 8654624	A	19860314	198743	
US 5181087	A	19930119	US 8717551	A	19870224	199306	
			US 89340471	A	19890419		
US 5373191	A	19941213	US 8717551	A	19870224	199504	
			US 89340471	A	19890419		
			US 92998856	A	19921230		
JP 8227990	A	19960903	JP 8641768	A	19860228	199645	
			JP 95340712	A	19860228		

Priority Applications (No Type Date): JP 8654624 A 19860314; JP 8641768 A 19860228; JP 95340712 A 19860228
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3706274	A		18		
US 5181087	A		20	H01L-029/80	Cont of application US 8717551
US 5373191	A		17	H01L-029/80	Cont of application US 8717551
					Cont of application US 89340471
					Cont of patent US 5181087
JP 8227990	A		5	H01L-029/778	Div ex application JP 8641768

Abstract (Basic): DE 3706274 A

Source and drain **electrode** metallisations of a FET with a deepened gate **electrode** metallisation are joined directly with a high-**impurity semiconductor** layer which faces the gate **electrode** and is separated from it by an **insulating layer** on the side walls of the **trench**. Source and drain **electrodes** can also be arranged to face the gate **electrode** directly, repeated just by the side insulation.

ADVANTAGE - This reduces the resistance between gate and the other **electrodes**, and the contact resistance between a **semiconductor** layer and source or drain, results in a lower **capacitance** of the deepened **gate**, and raises the source/gate breakdown voltage.

6a/15

Abstract (Equivalent): US 5373191 A

A **semiconductor device** having **multiple layers** with one metal **electrode** directly connected to one active layer of the device but isolated from another layer, provided on the active layer, by an air gap. The **electrode** is located inside a cut portion on the other layer with the air gap having a width corresp. to the spacing between the metal **electrode** and the other layer. The spacing being in the range 100-1000 Angstroms.

USE/ADVANTAGE - High performance cpd. effect **semiconductors** esp. field effect transistors. Source-gate breakdown voltage is increased and **electrode** capacitance is reduced by the air gap.

Dwg.6a/15

US 5181087 A

A 2-D FET comprises (a) a semi insulating GaAs substrate, (b) an undoped GaAs layer, (c) an undoped AlxGa1-xAs layer, (d) a **doped** AlyGa1-yAs layer, (e) an undoped AlzGa1-zAs layer 50-200 Angstroms thick, (f) a cap layer of high **dopant impurity** concn. having a recess for forming a gate **electrode**, (g) a source **electrode** on the cap layer and (h) a drain **electrode** on the cap layer. The gate **electrode** is disposed inside the recess and is isolated from the cap layer through an inorganic sidewall **insulator film** disposed only on the sidewall of the recess. x = 0.3-0.4, y = 0.2-0.4 and z = 0.3-0.4.

The sidewall **insulator film** is 100-1000 Angstroms thick. The cap layer is GaAs or Ge, with a **dopant impurity** concn. of 10 power (19) to 10 power (20) per cm3.

ADVANTAGE - High performance and easy mfr. Parasitic resistance between recessed and another **electrode** is considerably lowered. Capacitance of the recessed **electrode** is lowered so the source gate breakdown voltage is increased. (Dwg.6a/15

58/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013128181
WPI Acc No: 2000-300052/200026
XRAM Acc No: C02-080090
XRPX Acc No: N02-209858
Self-aligned heterojunction **bipolar transistor** includes metallic silicide layer formed on emitter layer and base **electrode**
Patent Assignee: KOREA ELECTRONICS & TELECOM RES INST (KOEL-N); KOREA ELECTRONICS & TELECOM RES (KOEL-N); ELECTRONICS & TELECOM RES INST (ELTE-N)
Inventor: CHO D H; HAN T H; LEE S M; YEOM B R; RYUM B R
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 99026266	A	19990415	KR 9748320	A	19970923	200026	B
US 6337494	B1	20020108	US 98137709	A	19980821	200232	
KR 275540	B	20001215	KR 9748320	A	19970923	200175	

Priority Applications (No Type Date): KR 9748320 A 19970923
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 99026266	A			H01L-029/70	
US 6337494	B1		20	H01L-031/0328	
KR 275540	B			H01L-029/70	Previous Publ. patent KR 99026266

Abstract (Basic): US 6337494 B1
Abstract (Basic):
NOVELTY - An **insulating film** (13) formed under the spacer (16), separates the emitter (14) from the **conductive layer** (11) of the base **electrodes** (12-1). A metallic silicide layer (17) is formed on the emitter and the base **electrodes**. The **insulating films** (9,10) and the **conductive layer** (11) are formed sequentially on the substrate (1) having a buried collector (2). A collector region (4) is formed by patterning the layers (9-11).
USE - Self-aligned heterojunction **bipolar transistor**.
ADVANTAGE - As the metallic silicide layer is formed on the emitter layer and the base **electrode**, the parasitic resistance of the base and the emitter is decreased. As the collector film is isolated from the others by **insulating film**, the use of sophisticated **trench** isolation process is eliminated, hence processing steps are reduced and manufacturing cost is increased. Since each of the self-alignments of base-collector and emitter-base are performed, the parasitic capacitance between the collector and the base is reduced, hence operating speed is enhanced.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the self-aligned **bipolar transistor**.
Substrate (1)
Buried collector (2)
Collector region (4)

Insulating layers (9,10)
Conductive layer (11)
Base **electrodes** (12-1)
Insulating film (13)
Emitter (14)
Spacer (16)
Metallic silicide layer (17)
pp; 20 DwgNo 5P/6

58/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009630502
WPI Acc No: 1993-324051/199341
XRAM Acc No: C96-010592
XRPX Acc No: N96-025994
High speed **semiconductor bipolar transistor** device - has metal region extending from collector **electrode** through n-type epitaxial layer to buried resistive layer while surrounded by n-**doped** amorphous silicon film with greater band gap
Patent Assignee: NEC CORP (NIDE)
Inventor: HASHIMOTO T; TASHIRO T
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 5235014	A	19930910	JP 9231223	A	19920219	199341	B
US 5475257	A	19951212	US 9321747	A	19930219	199604	
			US 94329992	A	19941027		

Priority Applications (No Type Date): JP 9231223 A 19920219
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 5235014	A		4	H01L-021/331	
US 5475257	A		11	H01L-023/48	Cont of application US 9321747

Abstract (Basic): US 5475257 A

The transistor device includes a p-type silicon substrate (1), a metal region (4), and a n-type **doped semiconductor** amorphous film (5). An n-plus resistive buried layer (2) lies over the silicon substrate and is itself overlayed by an n-type silicon epitaxial layer (3). **Trench** isolation regions (12) and an **insulation film** (8) are provided in and over the epitaxial layer.

The **trench** regions reach the silicon substrate. The metal region, e.g. of metal **multi-layer** tungsten/titanium, exists in the resistive buried layer and is directly under a collector **electrode** (9). The **semiconductor** film covers the plug and has a wider band gap than that of the buried layer. The film suppresses electrical current flow of carriers between the metal region and the buried layer.

ADVANTAGE - Allows high speed performance. Improves miniaturisation. N-type **doped** silicon film prevents majority carriers tunnelling from resistive and epitaxial layers to metal region and prevents short circuiting. Metal layer is replaceable with e.g. molybdenum.

Dwg.3/5

09/04/2002 09/986,277

60/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014668132
WPI Acc No: 2002-488836/200252
XRAM Acc No: C02-138810
XRPX Acc No: N02-386371
Semiconductor device has **multi-layer** of silicon nitride layer and silicon oxide layer formed on sidewalls and bottom of **trench** by atomic layer deposition
Patent Assignee: KIM D (KIMD-I); KIM Y (KIMY-I); LEE S (LEES-I); PARK Y (PARK-I)
Inventor: KIM D; KIM Y; LEE S; PARK Y
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020047151	A1	20020425	US 2001902607	A	20010712	200252	B

Priority Applications (No Type Date): KR 200061548 A 20001019
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020047151	A1		19	H01L-029/76	

Abstract (Basic): US 20020047151 A1
Abstract (Basic):
NOVELTY - A **semiconductor device** includes a **trench** (102) formed on **semiconductor** substrate (100); a liner **layer** (106) consisting of **multi-layer** of a silicon nitride layer and silicon oxide layer (104) formed on sidewalls and bottom of the **trench**; and a buried **insulating layer** (108) filled in the **trench** without void. The liner layer is formed by atomic layer deposition.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a method for fabricating a **semiconductor device**.
USE - Used as **semiconductor devices**.
ADVANTAGE - The invention maintains low thermal budget and prevents vacuum break.
DESCRIPTION OF DRAWING(S) - The figure is a sectional view of a **semiconductor device** having a thin film.
Substrate (100)
Trench (102)
Oxide layer (104)
Liner layer (106)
Gate stack pattern (118)
Gate spacers (122)
Bubble prevention layer (124, 140)
Insulating layer (126, 142)
pp; 19 DwgNo 6/11

60/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014510961
WPI Acc No: 2002-331664/200237
XRAM Acc No: C02-095839
XRPX Acc No: N02-260389
Formation of metallization and contact structures in integrated circuit (IC) involves forming **trench**, forming contact opening without damaging gate structure, and depositing **conductive** material into contact opening and **trench**
Patent Assignee: CYPRESS SEMICONDUCTOR CORP (CYPR-N)
Inventor: BLOSSE A; GILBOA Y; QIAO J; THEDKI S
Number of Countries: 028 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1168434	A2	20020102	EP 2001401542	A	20010614	200237	B
JP 2002016139	A	20020118	JP 2001181502	A	20010615	200237	
KR 2001113010	A	20011224	KR 200133430	A	20010614	200240	

Priority Applications (No Type Date): US 2000593967 A 20000615
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1168434	A2	E	17	H01L-021/768	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR				
JP 2002016139	A		12	H01L-021/768	
KR 2001113010	A			H01L-021/768	

Abstract (Basic): EP 1168434 A2
Abstract (Basic):
NOVELTY - Metallization and contact structures are formed in integrated circuit by:
(a) etching through **multiple layers** of **dielectric** materials to form **trench** without etching the contact **dielectric layer**;
(b) etching the contact **dielectric layer** under conditions which do not damage the gate structure to form a first contact opening; and
(c) depositing a **conductive** material into the contact opening and the **trench**.
DETAILED DESCRIPTION - Formation of metallization and contact structures in integrated circuit involves etching a **trench dielectric layer** (4) of a composite structure. The composite structure includes:
(i) a **semiconductor** substrate with an active region, a gate structure (3) and **dielectric spacers** adjacent the gate structure;
(ii) contact dielectric (1); and
(iii) **trench dielectric layer**.
Etching is carried out to form a **trench** (6) under etch conditions which do not etch the contact **dielectric layer**.

The process is followed by etching the contact **dielectric layer** under conditions which do not damage the gate structure to form a first contact opening (9) that exposes a region of the **semiconductor** substrate and a portion of the **dielectric spacer**(s), and depositing a **conductive** material into the contact opening and the **trench**.

USE - Forming metallization and contact structures in integrated circuit.

ADVANTAGE - The process increases device density and processing efficiency.

DESCRIPTION OF DRAWING(S) - The figure shows a **semiconductor** substrate after the **trench** and the contact opening are formed.

Contact dielectric (1)
Gate structure (3)
Trench dielectric layer (4)
Trench (6)
Contact opening (9)
pp; 17 DwgNo 7/10

60/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013858471
WPI Acc No: 2001-342684/200136
Related WPI Acc No: 2001-541203
XRAM Acc No: C01-105937
XRPX Acc No: N01-248169
Manufacture of dynamic random access memory cell involves forming transistor above capacitor node and lower **conductive** region, which are formed in vertical **trench** in dielectric stack of substrate surface
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: HORAK D V; MOHLER R L; STARKEY G S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6228706	B1	20010508	US 99384298	A	19990826	200136	B

Priority Applications (No Type Date): US 99384298 A 19990826
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6228706	B1		7	H01L-021/8242	

Abstract (Basic): US 6228706 B1
Abstract (Basic):

NOVELTY - Memory cell is manufactured by forming a transistor above a capacitor node and a lower **conductive** region which are formed in a vertical **trench** in a dielectric stack on a substrate surface. The transistor occupies a horizontal device area equal to that of a horizontal capacitor area occupied by the capacitor node and the lower **conductive** region.

DETAILED DESCRIPTION - Manufacture of memory cell containing a vertical transistor that is self-aligned with an underlying node **dielectric layer** comprises forming a vertical **trench** in a dielectric stack on a substrate surface and a substrate (10). A capacitor node (18) and a lower **conductive** region (20) in the vertical **trench** and occupying a horizontal capacitor area are formed. A transistor (24,26,28) is formed above the capacitor node and the lower **conductive** region. The transistor occupies a horizontal device area equal to that of the horizontal capacitor area. The transistor is formed by forming a surround gate near the periphery of the horizontal device area; forming an oxide layer on an inside surface of the surround gate; forming a **conductive** body inside the oxide layer; and forming diffusion regions in the **conductive** body near its top and bottom surfaces.

USE - For forming a dynamic random access memory cell.

ADVANTAGE - The method provides a memory cell having a reduced cell size and a design that is associated with high productivity.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of a memory cell.

substrate (10)
oxide layers (12,12',32)

nitride layers (14,30)
capacitor node (18)
lower **conductive** region (20)
transistor (24,26,28)
bitline (34)
pp; 7 DwgNo 1g/1

60/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011980323
WPI Acc No: 1998-397233/199834
XRAM Acc No: C98-120199
XRPX Acc No: N98-308976

Flash memory with floating bit line and manufacturing - by decreasing voltage difference between source and drain by channel program and channel erase to shrink bit line occupied area

Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO LTD (TASE-N)
Inventor: LIANG M; LIN R; SHYU C

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 325595	A	19980121	TW 97103070	A	19970312	199834	B

Priority Applications (No Type Date): TW 97103070 A 19970312
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 325595	A		38	H01L-027/10	

Abstract (Basic): TW 325595 A

Producing flash memory with floating bit line, which is applicable for forming matrix multiple flash memory cells on one first-type **semiconductor** substrate along one first orientation and one second orientation at predetermined angle with respect to the first orientation, comprises the following steps: (1) On the first-type **semiconductor** substrate in sequence forming one second- type layer and one first-type layer; (2) Along the first orientation individually forming multiple isolating **trenches** deep to the second-type layer, and isolating said first-type **layer** into **multiple** body lines; (3) On the isolating **trench** forming insulator; (4) On the body line in sequence forming first **dielectric** and first **conductive layer**; (5) On the first **conductive layer** in sequence forming one second dielectric and one second **conductive layer**; (6) Along the second orientation etching to said body line so as to form stacked gate of the multiple flash memory cells, and control gate of the stacked gate extends along the second orientation to become word line; (7) With the stacked gate as mask, **doping** second-type **dopant** to the body line to form second-type **doped** region, therefore forms drain and source region of the flash memory cell; (8) Lateral side of the stacked gate forming **insulating spacer**; (9) On the second-type **doped** regions between the **insulating spacers** independently forming bit lines.

60/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011500913
WPI Acc No: 1997-478826/199744
XRAM Acc No: C97-152009
XRPX Acc No: N97-399407

Manufacturing stack capacitor of dynamic random access memory - with increased capacitor **electrode** area and larger capacitance

Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)
Inventor: SHYU J; HSU C
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 311258	A	19970721	TW 97100813	A	19970124	199744	B
US 5902123	A	19990511	US 97953239	A	19971017	199926	

Priority Applications (No Type Date): TW 97100813 A 19970124
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 311258	A		11	H01L-021/70	
US 5902123	A			H01L-021/8242	

Abstract (Basic): TW 311258 A

Manufacturing stack capacitor of dynamic random access memory comprises: (1) supplying one silicon substrate, in which the silicon substrate has one field oxide, one metal oxide **semiconductor device** and one insulator with one contact; (2) forming multiple **doped** polysilicon and **multiple** WSi **layers** above the substrate, in which those **doped** polysilicon and those WSi layers are formed in interlaced stack; (3) patterning those **doped** polysilicon and those WSi layers to form bottom plate of the stack capacitor; (4) selectively etching those **doped** polysilicon and those WSi layers, so as to form multiple **trenches** on those **doped** polysilicon and those WSi layer sides, thereby increasing bottom plate area; (5) forming one dielectric above those **doped** polysilicon and those WSi surface; (6) forming one **conductive layer** on the **dielectric** surface to form top plate of the stack capacitor, therefor forming stack capacitor of the dynamic random access memory.

Dwg.1/2

60/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011186043
WPI Acc No: 1997-163968/199715
XRPX Acc No: N97-135064
Process of capacitor element of DRAM - forming **electrode** structure with **multi-layer** fins to increase capacitance
Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)
Inventor: HWANG H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 293930	A	19961221	TW 96102011	A	19960216	199715	B

Priority Applications (No Type Date): TW 96102011 A 19960216
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 293930	A			H01L-021/31	

Abstract (Basic): TW 293930 A

A process of capacitor element of DRAM comprises of the following steps: (1) supplying one **semiconductor** substrate with formed field oxide, transistor element and one insulator with contact opening; (2) on the insulator alternatively forming multiple polysilicon and insulator space to form one stacked structure, in which the most bottom polysilicon has implanted **impurity** to increase conductivity, and via the contact opening connecting with the **semiconductor** substrate; (3) alternatively etching the insulating space with stacked structure and polysilicon until to the most bottom polysilicon surface for forming one opening; (4) by wet etching insulating polysilicon in the opening a distance toward inner, making the opening side wall have multiple **trenches**; (5) forming one second polysilicon overlaying on the above multiple **insulating spacers** and exposed surface of polysilicon; (6) etching the second polysilicon and every layer with stacked structure to define capacitor element range, in which the second polysilicon connects each polysilicon of the stacked structure to constitute bottom plate of the capacitor element; (7) removing each **insulating spacer** of the stacked structure to leave bottom plate of the capacitor element; (8) by using one thermal treatment process in sequence forming one dielectric overlaying on **electrode** surface under the capacitor element, meantime **impurity** inside the most bottom polysilicon, via the contact opening, also diffuses to the **semiconductor** substrate to form one contact region; and (9) forming one third polysilicon overlaying the dielectric surface as top plate of the capacitor element, finishing the capacitor element process.

60/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010999433
WPI Acc No: 1996-496382/199649
XRAM Acc No: C96-155069
XRPX Acc No: N96-418677
DRAM capacitor prodn. - includes forming insulator on **semiconductor** substrate, forming **multiple** polysilicon **layers** on **insulator**, forming **trench** through substrate, etc.
Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)
Inventor: HORNG Y; JENG J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 282579	A	19960801	TW 95106404	A	19950621	199649	B

Priority Applications (No Type Date): TW 95106404 A 19950621
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 282579	A		17	H01L-021/108	

Abstract (Basic): TW 282579 A

DRAM capacitor prodn. comprises: (i) forming an insulator on a **semiconductor** substrate; (ii) forming **multiple** polysilicon **layers** on the **insulator**, where the **doped** density of the odd layers in the polysilicon is different from the even layers; (iii) forming a deep **trench** through the substrate, through one of the polysilicon layers and either of the drain or source of the MOS transistor; (iv) forming a polysilicon on the **trench** and polysilicon; (v) forming a masking layer on the polysilicon to confine the **conductive layer** of the capacitor; with the masking layer used in plasma etching of the polysilicon, and due to the different **doped** density of either the odd or even layer in the polysilicon isotropic etching or anisotropic etching to make the polysilicon form the a down **conductive layer**; (vi) removing the masking layer; and (vii) forming a dielectric of the capacitor on the down **conductive layer** surface.

USE - Used as a capacitor on a **semiconductor** substrate with a formed MOS transistor.

Dwg.0/3

60/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008190045
WPI Acc No: 1990-077046/199011
XRPX Acc No: N90-059191
Semi-**conductive** crystalline element magnetic field sensor - has **multi-layer doping** superlattice of material of short carrier recombination time and high carrier mobility
Patent Assignee: GENERAL MOTORS CORP (GENK)
Inventor: HEREMANS J P; PARTIN D L
Number of Countries: 010 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 358322	A	19900314	EP 89307773	A	19890731	199011	B
US 4926226	A	19900515	US 88240778	A	19880906	199024	
JP 2121378	A	19900509				199025	
EP 358322	B1	19941026	EP 89307773	A	19890731	199441	
DE 68919036	E	19941201	DE 619036	A	19890731	199502	
			EP 89307773	A	19890731		
ES 2062008	T3	19941216	EP 89307773	A	19890731	199505	
SG 9590775	A	19951222	SG 9590775	A	19950428	199611	

Priority Applications (No Type Date): US 88240778 A 19880906
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 358322	A	E	9		
Designated States (Regional): DE ES FR GB IT NL SE					
EP 358322	B1	E	12	H01L-029/82	
Designated States (Regional): DE ES FR GB IT NL SE					
DE 68919036	E			H01L-029/82	Based on patent EP 358322
ES 2062008	T3			H01L-029/82	Based on patent EP 358322
SG 9590775	A				Previous Publ. patent EP 358322

Abstract (Basic): EP 358322 A

An integrated pair of magnetodiodes (30,40) separated by a V-shaped **trench** (50), is formed by epitaxial growth of the required number of **layers** on a semi-**insulating** substrate (52). A series of separate regions (54) of short carrier recombination times is provided along the walls of the **trench**. These are formed using an apertured mask along the **trench** and unannealed ion implantation to damage selectively the unmasked regions, forming the required regions of short recombination time.

Spacing apart the regions of short carrier recombination time avoids the risk of forming a shorting **conductive layer**. The outer surfaces (35,45) of the diodes (30,40) are treated by proton bombardment to maintain long recombination lifetimes.

USE/ADVANTAGE - Magneto diodes for position-sensing in automotive applications are provided which have relatively high sensitivity to magnetic field.

3B/3

Abstract (Equivalent): EP 358322 B

A magnetic field sensor comprising a semi-**conductive** crystalline element (11;52) which comprises a **doping** superlattice of a plurality of layers formed by an n-i-p-i superstructure of a semi-**conductive** material which displays, in bulk, a relatively short carrier recombination time but a high carrier mobility; injecting **electrodes** (18,19;32,34,42,44) along respective opposed faces of the element (11;52) to contact respective opposite ends of each of the layers (12,14); and where each of the layers (12;14) contains at least one region (26;30;40) of long carrier recombination times adjacent at least one region (24;54) of short carrier recombination times so that carriers are deflected between the regions of short and long carrier recombination times by a magnetic field to be sensed.

Dwg.1/3b

Abstract (Equivalent): US 4926226 A

The magnetic field sensor comprises a **semiconductive** crystalline element that includes at least one region of long carrier recombination times adjacent at least one region of short carrier recombination times for deflection of carriers between the regions of short and long carrier recombination times by a magnetic field to be sensed. The **semiconductive** element comprises a **doping** superlattice of a number of layers formed by an n-i-p-i superstructure of a **semiconductive** material of a relatively short carrier recombination time in bulk but of a high mobility, and each layer has a thickness less than the Debye length of charge carriers in such layer.

ADVANTAGE - Improved mobility.

Increased recombination times.

(8pp

60/3,AB/9 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06691701
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 2000-277531 [JP 2000277531 A]
PUBLISHED: October 06, 2000 (20001006)
INVENTOR(s): INAGAWA HIROMI
MACHIDA NOBUO
OISHI KENTARO
APPLICANT(s): HITACHI LTD
HITACHI ULSI SYSTEMS CO LTD
APPL. NO.: 11-081667 [JP 9981667]
FILED: March 25, 1999 (19990325)

ABSTRACT

PROBLEM TO BE SOLVED: To prevent the occurrence of a source offset by forming a **trench** gate **conductor layer** and a gate **insulating film** in a **trench** and on the main surface of the periphery of the **trench** in a **semiconductor device** having a FET of a **trench** gate structure, in which a **conductor** to be a gate is provided in a **trench** extending on the main surface of a **semiconductor** substrate.

SOLUTION: A **trench** gate 4 of a MISFET of this type is formed in a **trench** extending to an n-type second **semiconductor** layer 2a to be a drain region from the main surface of a **semiconductor** substrate via a **multi-layer** gate **insulating film** 5 formed of a thermal oxide film and a deposition film, and is formed of polycrystalline silicon **doped** with **impurities**, for example. The top surface of the **trench** gate 4 is higher than the surface of a third **semiconductor** layer 2c to be a source region, that is, the main surface of the **semiconductor** substrate. Therefore, this can prevent the **trench** gate 4 from being off the source region, that is, a source offset, even if the source region is made shallow. It is desirable that the top surface of the **trench** gate 4 is formed almost flat or convexly.

60/3,AB/10 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03361856
SEMICONDUCTOR DEVICE

PUB. NO.: 03-024756 [JP 3024756 A]
PUBLISHED: February 01, 1991 (19910201)
INVENTOR(s): TSUDA KATSUNORI
APPLICANT(s): SHARP CORP [000504] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-160503 [JP 89160503]
FILED: June 22, 1989 (19890622)
JOURNAL: Section: E, Section No. 1056, Vol. 15, No. 148, Pg. 106, April 15, 1991 (19910415)

ABSTRACT

PURPOSE: To develop a large capacitance in a limited shared area subjected to the least crystal defect by a method wherein a **semiconductor device** is provided with the first **electrode** in at least a part of regions on the surfaces of **multiple** patterned **conductor films**, an **insulating film** formed on the first **electrode** and the second **electrode** formed on the **insulating film**.

CONSTITUTION: The first **electrode** has **impurity** diffused layer 2 formed in specific regions on the surface of a single crystal silicon substrate 1 as well as **multiple** pattered polycrystal silicon **films** 3 while an Si(sub 3)N(sub 4) film 4 as a capacitance **insulating film** is formed on the first **electrode** and then an Al-Si wiring 5 as the second **electrode** is formed on the Si(sub 3)N(sub 4) film 4. Accordingly, the surface area of the first **electrode** can be notably increased by the side area of patterned polycrystal films 3. Through these procedures, the capacitor capacity can be increased to the value required for circuit design in a limited small shared area while the development of crystal defect due to **trenches** in the single crystal silicon substrate 1 can be avoided since there is no deeply formed **trenches** at all.

04sep02 11:40:28 User267149 Session D303.1

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File 315:ChemEng & Biotec Abs 1970-2002/Jul
(c) 2002 DECHEMA

Set	Items	Description
S1	32570	AU=(TAKAHASHI, H? OR TAKAHASHI H?)
S2	883	S1 AND SEMICONDUCT?????
S3	4	S2 AND (MULTIPLE OR MULTI)(3N)(LAYER???? OR COAT?????? OR FILM???????)
S4	4	RD (unique items)
S5	879	S2 NOT S3
S6	25	S5 AND (TRENCH???????? OR DITCH???? OR FURROW????)
S7	4	S6 AND (ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT????)
S8	4	RD (unique items)
S9	21	S6 NOT S8
S10	18	S9 AND (TIGBT OR CSTBT OR CARRIER()STORED()TRENCH OR IGBT OR GATE()BIPOLAR()TRANSISTOR? ?)
S11	0	S10 AND (DOPE???? OR DOPA???? OR DOPE???? OR DOPA?????? OR DOPING OR IMPURIT???????)
S12	15	RD S10 (unique items)
S13	3	S9 NOT S10
S14	3	RD (unique items)
S15	854	S5 NOT S6
S16	122	S15 AND (DOPE???? OR DOPA???? OR DOPE???? OR DOPA?????? OR DOPING OR IMPURIT???????)
S17	1	S16 AND (BIP()TR OR BIPOLAR()TRANSISTOR)
S18	121	S16 NOT S17
S19	2	S18 AND ((INSULAT?????? OR DIELECTRIC???)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR SPACER???))
S20	119	S18 NOT S19
S21	0	S20 AND ((CONTROL OR MAIN)(3N)(ELECTRODE? ? OR MICROELECTRODE? ? OR CONDUCT????))
S22	0	S20 AND ((GATE? ? OR OPENING? ?)(3N)(CAPACIT??????? OR CONDENS????))

4/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7074118 INSPEC Abstract Number: B2001-12-0170J-025
Title: Superior structure build-up substrate, "Advanced DV-MULTI" for packaging
Author(s): Sumi, S.; Nakamura, H.; **Takahashi, H.**
Author Affiliation: Dev. Dept, NEC Toyama Ltd., Japan
Conference Title: Pan Pacific Microelectronics Symposium. Proceedings of the Technical Program p.448-52
Publisher: Surface Mount Technol. Assoc, Edina, MN, USA
Publication Date: 2001 Country of Publication: USA 520 pp.
Material Identity Number: XX-2000-03037
Conference Title: Proceedings of 6th Annual Pan Pacific Microelectronics Symposium
Conference Sponsor: IMAPS; ITRI; Japan Inst. Electron. Packaging, Semicond. Equipment & Mater. Int.; et al
Conference Date: 13-16 Feb. 2001 Conference Location: Kauai, HI, USA
Language: English
Abstract: Since 1996, NEC have provided a build-up PWB named "DV-**MULTI** (Dimple Via-**MULTI layer** boards)", which is an ultra high-density build-up substrate with excellent reliability for high-density devices, e.g. bare chip, CSP, etc. However, **semiconductor** packaging customers require these build-up substrates with higher reliability performances and with more circuitry. Therefore, we have evolved the "Advanced DV-MULTI" by improving the additive electroless Cu plating process, the new permanent photoresist and insulation layer materials, and the high accuracy UV-YAG laser ablation process. Technologies for 20 mu m line and space patterns and 40 mu m diameter vias have been obtained from the new permanent photoresist, the refined additive electroless Cu plating solution and use of the high accuracy UV-YAG laser system. The permanent photoresist is resistant to the alkaline electroless Cu plating solution. We can control permanent photoresist height using a spin coater system. The UV-YAG laser has superior performance, such as via placement accuracy within +or-3 mu m, high throughputs of 500 holes/sec (50 mu m diameter) and via diameter range of 40 mu m to 80 mu m. Insulation materials have special electrical, thermal and mechanical properties. The dielectric constant (at 1 MHz) is 3.7 and loss tangent (at 1 MHz) is 0.020. The glass transition temperature is 170 degrees C (Futonagane and Takahashi, 1997; Maniwa, 1998).
Subfile: B

4/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7053159 INSPEC Abstract Number: B2001-11-2550E-017
Title: Surface passivation of epitaxial **multi-layer** structures for InP-based high speed devices by an ultrathin silicon layer
Author(s): Yong-Gui Xie; Takahashi, K.; **Takahashi, H.**; Jiang Chao; Kasai, S.; Hasegawa, H.
Author Affiliation: Res. Center for Integrated Quantum Electron., Hokkaido Univ., Sapporo, Japan
Journal: Transactions of the Institute of Electronics, Information and Communication Engineers C vol.J84-C, no.9 p.872-82
Publisher: Inst. Electron. Inf. & Commun. Eng,
Publication Date: Sept. 2001 Country of Publication: Japan
CODEN: DJTCEX ISSN: 1345-2827
SICI: 1345-2827(200109)J84C:9L.872:SPEM;1-0
Material Identity Number: K840-2001-009
Language: Japanese
Abstract: A novel surface passivation technique of epitaxial **multi-layer** structures for InP-based high speed devices by an ultrathin silicon interface control layer (Si ICL) is discussed. Firstly, theoretical design and optimization of the surface passivation structure with and without an InGaAs cap layer is made by taking account of the strain effect and quantized states in the ultrathin Si ICL. Then the formation process of SiN/sub x//Si ICL structure utilizing a novel partial-nitridation technique is optimized. It is clarified that the InGaAs cap layer is important for the Si ICL-based surface passivation on InP-based materials. The planar metal-insulator-**semiconductor** (MIS) diode is studied to characterize the I-S interface of the devices fabricated on semi-insulating InP substrates, which shows that the Si ICL technique is useful for the surface passivation of InP-based **multi-layer** structures.
Subfile: B

4/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

5884550 INSPEC Abstract Number: A9810-8265-034
Title: Chemical reactions and electronic functions of carbon cluster arrays studied by scanning tunneling spectroscopy and high-resolution electron energy loss spectroscopy
Author(s): Kasuya, A.; Hu, C.-W.; Suto, S.; Tohji, K.; **Takahashi, H.**; Czajka, R.; Wawro, A.; Nishina, Y.
Author Affiliation: Inst. of Mater. Res., Tohoku Univ., Sendai, Japan
Journal: Acta Physica Polonica A Conference Title: Acta Phys. Pol. A (Poland) vol.93, no.2 p.317-22
Publisher: Inst. Phys. Polish Acad. Sci,
Publication Date: Feb. 1998 Country of Publication: Poland
CODEN: ATPLB6 ISSN: 0587-4246
SICI: 0587-4246(199802)93:2L.317:CREF;1-X
Material Identity Number: A184-98003
Conference Title: 1st International Symposium on Scanning Probe Spectroscopy and Related Methods, SPS '97
Conference Date: 15-18 July 1997 Conference Location: Poznan, Poland
Language: English
Abstract: Novel nanometer scale structures have been produced by thermal heating or laser irradiation on the surface of single- and **multi-layers** of C/sub 60/ and C/sub 84/ on Si. These structures were examined by combined measurements of scanning tunneling spectroscopy and high resolution electron energy loss spectroscopy. The results show specific chemical reactions of the substrate with carbon clusters having single- and double-bonded network. Covalent bonds are formed in some of these chemical reactions.
Subfile: A

4/3,AB/4 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

05063333 JICST ACCESSION NUMBER: 01A0889787 FILE SEGMENT: JICST-E
Surface Passivation of Epitaxial **Multi-Layer** Structures for InP-Based High Speed Devices by an Ultrathin Silicon Layer.
XIE Y-G (1); CHAO J (1); KASAI SEIYA (1); HASEGAWA HIDEKI (1); TAKAHASHI KEN (2); **TAKAHASHI HIROSHI** (2)
(1) Hokudai Shusekikaimen'erekutoronikusukense; (2) Hokkaido Univ., Graduate School of Engineering, JPN
Denshi Joho Tsushin Gakkai Ronbunshi C(Transactions of the Institute of Electronics, Information and Communication Engineers C), 2001, VOL.J84-C,NO.9, PAGE.872-882, FIG.11, REF.22
JOURNAL NUMBER: S0623CAH ISSN NO: 1345-2827
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: By carrying out fundamental investigation on a method to perform surface inactivation of InAlAs/InGaAs/InAlAs/InP **multi layer** epitaxial thin **film** structure used for preparation of InP series fast device by using superthin film silicon interface control layer (Si ICL), new informations on following three points could be obtained. (1) On cases with and without InGaAs cap layer on its surface, by considering strain effect and quantum state control, theoretical design and optimization of inactivation structure were carried out. (2) By carrying out investigation on a process to realize a designed inactivation structure, together with performing formation of Si ICL and optimization of formation condition of SiN(sub x)/Si ICL, importance of InGaAs cap layer was experimentally elucidated. And, (3) On surface inactivation structure due to optimal process, interface electronic physics of **multi layer** thin **film** MIS structure by using planar type MIS capacity element capable of preparing onto the same insulation substrate as that of device was evaluated, to prove effectiveness of Si ICL.

09/04/2002 09/896,161

8/3,AB/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04049400
E.I. No: EIP95012524433
Title: 600V **trench** IGBT in comparison with planar IGBT - an evaluation of the limit of IGBT performance -
Author: Harada, M.; Minato, T.; **Takahashi, H.**; Nishihara, H.; Inoue, K.; Takata, I.
Corporate Source: Mitsubishi Electric Corp, Mizuhara Itami city, Jpn
Conference Title: Proceedings of the 1994 6th IEEE International Symposium on Power Semiconductor Devices & ICs
Conference Location: Davos, Switz Conference Date: 19940531-19940602
E.I. Conference No.: 42306
Source: IEEE International Symposium on Power Semiconductor Devices & ICs 1994. p 411-416
Publication Year: 1994
CODEN: 001709
Language: English
Abstract: We have developed a large area **trench** MOS process and experimentally manufactured a 600V, 50A class **trench** IGBT. Narrowing the **trench** pitch, those devices got better ON state voltage(V//C//E(sat) equals 1.4V, t//f equals 230ns @200A/cm**2) and much better endurance property(dI//c/dt approximately equals 2500A/(s center dot cm**2)) for latch-up than planar IGBTs. **Trench** IGBTs also showed higher breakdown voltage(BV//C//E//S) than planar IGBTs. We had confirmed that **trench** IGBT realizes the ideal structure, 'pin diode plus MOS gate', which was proposed at the start of the developing IGBT. The **trench** IGBT would be expected as a superior high voltage device, especially due to its endurance property for latch-up operation. (Author abstract) 10 Refs.

09/04/2002 09/896,161

8/3,AB/2 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03049860 JICST ACCESSION NUMBER: 96A0919269 FILE SEGMENT: JICST-E
Carrier Stored **Trench**-Gate Bipolar Transistor(CSTBT).
TAKAHASHI HIDEKI (1); HAGINO HIROYASU (1); YAMADA TOMIHISA (1);
TOMINAGA SHUICHI (2)
(1) Mitsubishi Electr. Corp.; (2) Fukuryosemikon'enjiniaringu
Denki Gakkai Denshi Debaisu Kenkyukai Shiryo, 1996, VOL.EDD-96,NO.101-115,
PAGE.61-67, FIG.10, REF.7
JOURNAL NUMBER: Z0910AAZ
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: A new device concept, called the Carrier Stored Trernch-Gate Bipolar Transistor(CSTBT) is reported for the first time. The CSTBT forms the n layer under p base between **trenches**, the n layer store carriers in n- layer, as result, the carrier distribution of the CSTBT become that of the diode. We examined the performance of the CSTBT by the simulation and the experiment in the case of the blocking voltage is 1700V, compared to the simple **Trench** IGBT(TIGBT) and the PiN diode, confirmed the CSTBT is superior to the TIGBT, and the on-state voltage of the CSTBT almost same to the Vf of the PiN diode. By the fabricated CSTBT, on-state voltage is 1.9V at 50A/cm2, turn-off time of resistive load switching is about 300nsec. Further we realized turn-off current capability of the CSTBT is about 300A/cm2. (author abst.)

8/3,AB/3 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02252820 JICST ACCESSION NUMBER: 94A0879344 FILE SEGMENT: JICST-E
The development of IGBT modules for battery forklifts.
KANEZAWA KEN'ICHI (1); **TAKAHASHI HIDEKI** (1); YU YOSHINORI (1); KOURA MASAYUKI (2); INOUE MASAKI (2)
(1) Mitsubishi Electr. Corp., Fukuoka Work.; (2) Fukuryosemikon'enjiniaringu
Denki Gakkai Denshi Debaisu Kenkyukai Shiryo, 1994, VOL.EDD-94,NO.29-35.37-38, PAGE.35-42, FIG.12, TBL.1, REF.3
JOURNAL NUMBER: Z0910AAZ
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: We developed a new IGBT that uses **trenched** gates. In the new IGBT, current flows directly from the emitter to the collector which makes for easy cell processing. The unit cell could be reduced to 1/10 of conventional ones in size, allowing for a reduction in the "on" voltage. The rated current of IGBT modules using this is a very low VCE(SAT)=1.2V.The power loss of the chopper operating conditions is also 35% less than that for the bi-polar transistor module.

09/04/2002 09/896,161

8/3,AB/4 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02252648 JICST ACCESSION NUMBER: 94A0868874 FILE SEGMENT: JICST-E
600V **trench** IGBT.(I).(trial manufacture result).
NISHIHARA HIDENORI (1); **TAKAHASHI HIDEKI** (1); INOUE KEIJI (1); HARADA MASANA (1); MINATO TADANORI (1)
(1) Mitsubishi Electr. Corp.
Denki Gakkai Denshi Debaisu Kenkyukai Shiryo, 1994, VOL.EDD-94,NO.39-49, PAGE.77-83, FIG.13, REF.5
JOURNAL NUMBER: Z0910AAZ
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: As a result of manufacturing the **trench** IGBT rated at 600V, 50A, we managed to achieve a large reduction in the size of the 3rd generation flat IGBT as well as in improvement in the trade-offs. The on-state voltage characteristics of this IGBT are limited to mass-produced IGBTs.
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09/04/2002 09/896,161

12/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7092154 INSPEC Abstract Number: B2001-12-2560P-020
Title: Wide cell pitch 1200 V NPT CSTBTs with short circuit ruggedness
Author(s): Nakamura, H.; Nakamura, K.; Kusunoki, S.; **Takahashi, H.**; Tomomatsu, Y.; Harada, M.
Author Affiliation: Mitsubishi Electr. Corp., Kumamoto, Japan
Conference Title: Proceedings of the 13th International Symposium on Power Semiconductor Devices & ICs. IPSD '01 (IEEE Cat. No.01CH37216) p. 299-302
Publisher: Inst. Electr. Eng. Japan, Tokyo, Japan
Publication Date: 2001 Country of Publication: Japan xxxi+467 pp.
ISBN: 4 88686 056 7 Material Identity Number: XX-2001-01446
Conference Title: Proceedings of the 13th International Symposium on Power Semiconductor Devices & ICs. IPSD '01
Conference Sponsor: Inst. Electr. Eng. Japan
Conference Date: 4-7 June 2001 Conference Location: Osaka, Japan
Language: English
Abstract: We have studied a suitable structure for 1200 V NPT-IGBTs from the viewpoint of total performance. We propose the wide cell pitch **CSTBT** (**Carrier Stored Trench** Bipolar Transistor) structure. As a result, small gate capacitance and short circuit ruggedness have been established by reducing MOS channel width. A small on-state voltage has been achieved by the carrier store effect of CSTBTs. To control the breakdown voltage and to suppress oscillation during short circuit operation, damping **trench** capacitors have been also prepared.
Subfile: B

09/04/2002 09/896,161

12/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6605596 INSPEC Abstract Number: B2000-07-1210-004
Title: New generation 1200 V power module with **trench** gate **IGBT** and super soft recovery diode and its evaluations
Author(s): Lwamoto, H.; Kawakami, A.; Satoh, K.; **Takahashi, H.**; Nakaoka, M.
Author Affiliation: Mitsubishi Electr. Co., Fukuoka, Japan
Journal: IEE Proceedings-Electric Power Applications vol.147, no.3 p.153-8
Publisher: IEE,
Publication Date: May 2000 Country of Publication: UK
CODEN: IEPAER ISSN: 1350-2352
SICI: 1350-2352(200005)147:3L.153:G1PM;1-A
Material Identity Number: B477-2000-003
U.S. Copyright Clearance Center Code: 1350-2352/2000/$20.00
Language: English
Abstract: A 1200 V **IGBT** with **trench** gate and punch through structures is developed on the basis of simulation and experimental analyses. Both results of simulation and measurement of the prototype device have good agreement. Though the chip area of the new **IGBT** is about 30-50% smaller than that of the conventional **IGBT** , the saturation voltage is about 30-40% lower, the switching loss is also about 20%, smaller than those of conventional **IGBT**, respectively, and the new **IGBT** has a larger reverse bias safe operating area (RBSOA). Capability to withstand short circuits is achieved by a new current limiting circuit. In addition, a fast switching diode with an excellent soft recovery characteristic is practically developed by using local lifetime control processing in the anode side n-layer. As an experimental result, its power dissipation, spike surge voltage and electromagnetic noise can be lowered. The structures and characteristics of the developed **IGBT** , diode and power module are presented, and their analytical results are discussed and evaluated from a practical and an applications point of view.
Subfile: B

12/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6582642 INSPEC Abstract Number: B2000-06-2560R-049
Title: Features and application of new 1200 V **trench** gate **IGBT** modules
Author(s): Iwamoto, H.; Tabata, M.; **Takahashi, H.**; Thal, E.; Wheeler, N.
Author Affiliation: Power Device Div., Mitsubishi Electr. Corp., Fukuoka, Japan
Conference Title: PCIM'99. Europe. Official Proceedings of the Thirty-Ninth International Power Conversion Conference p.227-31
Publisher: ZM Commun. GMBH, Nurnberg, Germany
Publication Date: 1999 Country of Publication: Germany xiv+705 pp.
ISBN: 3 928643 22 3 Material Identity Number: XX-2000-00435
Conference Title: PCIM'99 Europe Official Proceedings of the Thirty-Ninth International Power Conversion Conference
Conference Date: 22-24 June 1999 Conference Location: Nurnberg, Germany
Language: English
Abstract: A new type of 1200 V **IGBT** has been developed, using a **trench** gate structure and local lifetime control. This device has 20-30% lower losses than planar IGBTs in a typical application. The **IGBT** technology is complemented by a super-soft recovery freewheel diode, and a new package design with low inductance and low stray capacitance. The resulting low-loss, low-noise module has the potential to reduce the size and overall system cost of power conversion equipment. Integrated active current clamping gives a short circuit withstand capability equal to planar IGBTs, and can enhance system reliability by simplifying protection against short circuits.
Subfile: B

12/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6475113 INSPEC Abstract Number: B2000-02-2560R-089
Title: New 1200 V power modules with sophisticated **trench** gate **IGBT** and superior soft recovery diode
Author(s): Iwamoto, H.; **Takahashi, H.**; Tabata, M.; Satoh, K.
Author Affiliation: Power Device Div., Mitsubishi Electr. Corp., Fukuoka, Japan
Conference Title: Proceedings of the IEEE 1999 International Conference on Power Electronics and Drive Systems. PEDS'99 (Cat. No.99TH8475) Part vol.1 p.28-33 vol.1
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA 2 vol. xxviii+1173 pp.
ISBN: 0 7803 5769 8 Material Identity Number: XX-1999-00962
U.S. Copyright Clearance Center Code: 0 7803 5769 8/99/$10.00
Conference Title: Proceedings of Third IEEE International Conference on Power Electronics and Drive Systems (PEDS'99)
Conference Sponsor: IEEE Singapore Section; Univ. of Hong Kong; City Univ of Hong Kong; Hong Kong Univ. of Sci. & Technol.; Hong Kong Tech. Coll
Conference Date: 27-29 July 1999 Conference Location: Hong Kong
Language: English
Abstract: A new PT-type **trench** gate **IGBT** has been developed using a local lifetime control in the n+ buffer layer. A prototype was developed after analyzing the device and estimating its characteristics using simulation. Both the result of simulation and that of measurement of the prototype have matched. Though the chip area is about 40~50% smaller than the conventional **IGBT**, the newly developed **IGBT**'s on-state voltage is about two-thirds (1.8 V, typically), its switching loss is about 80%, and has a larger reverse bias switching withstand capability. Also, a high-speed diode with excellent soft recovery characteristic was developed using local lifetime control in anode-side n-layer. As a result, a reduction of surge voltage, noise, and switching power loss has been achieved. This paper presents the structures and characteristics of the new **IGBT** and diode and their analysis results.
Subfile: B

12/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

6425707 INSPEC Abstract Number: B2000-01-2560R-064
Title: Local lifetime control and punch-through structure cut V/sub CE(sat)/
Author(s): Motto, E.R.; Donlon, J.F.; **Takahashi, H.**; Tabata, M.
Author Affiliation: Powerex Inc., Youngwood, PA, USA
Journal: PCIM Power Electronic Systems vol.25, no.7 p.46, 48-9, 51-2, 55-6
Publisher: Adams/Intertec International,
Publication Date: July 1999 Country of Publication: USA
CODEN: PPESFB ISSN: 0885-0259
SICI: 0885-0259(199907)25:7L.46:LLCP;1-V
Material Identity Number: H278-1999-006
Language: English
Abstract: The authors describe a new 1200V punchthrough **trench** gate **IGBT** with local lifetime control which sets a V/sub CE(sat)/ benchmark of 1.9V at 140A/cm2, T/sub j/=125 degrees C. Optimized packaging and a new freewheel diode also improve module performance.
Subfile: B

12/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

5392012 INSPEC Abstract Number: B9611-2560J-025
Title: **Carrier stored trench-gate bipolar transistor** (**CSTBT**)-a novel power device for high voltage application
Author(s): **Takahashi, H.**; Haruguchi, H.; Hagino, H.; Yamada, T.
Author Affiliation: Power Device Div., Mitsubishi Electr. Corp., Fukuoka, Japan
Conference Title: 8th International Symposium on Power Semiconductor Devices and ICs. ISPSD '96 Proceedings (Cat. No.96CH35883) p.349-52
Editor(s): Salama, C.A.T.; Williams, R.K.
Publisher: IEEE, New York, NY, USA
Publication Date: 1996 Country of Publication: USA 362 pp.
ISBN: 0 7803 3106 0 Material Identity Number: XX96-01778
U.S. Copyright Clearance Center Code: 0 7803 3106 0/96/$5.00
Conference Title: 8th International Symposium on Power Semiconductor Devices and ICs. ISPSD '96. Proceedings
Conference Sponsor: IEEE Electron Devices Soc.; IEE of Japan
Conference Date: 20-23 May 1996 Conference Location: Maui, HI, USA
Language: English
Abstract: A new device concept, called the **Carrier Stored Trench-Gate Bipolar Transistor** (**CSTBT**) is reported for the first time. The **CSTBT** forms the n layer under p base between **trenches**, the n layer stores carriers; as aesult, the carrier distribution of the **CSTBT** becomes that of the diode. We examined the performance of the **CSTBT** by simulation and experiment in the case of the blocking voltage of 1700 V, compared to the simple **trench IGBT** (**TIGBT**) and the PiN diode. This confirmed the **CSTBT** is superior to the **TIGBT**, and the on-state voltage of the **CSTBT** is almost same as the Vf of the PiN diode. By the fabricated **CSTBT** , on-state voltage is 1.9 V at 50 A/cm/sup 2/, turn-off time of resistive load switching is about 300 nsec. We realized turn-off current capability of the **CSTBT** above 250 A/cm/sup 2/.
Subfile: B

12/3,AB/7 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05930457
E.I. No: EIP01446710208
Title: 600v **CSTBT** having ultra low on-state voltage
Author: **Takahashi, H.**; Aono, S.; Yoshida, E.; Moritani, J.; Hine, S.
Corporate Source: Mitsubishi Electric Corporation ULSI Development Center, Fukuoka-City, Fukuoka 819-01, Japan
Conference Title: 13th International Symposium on Power Semiconductor Devices and ICs (ISPSD'01)
Conference Location: Osaka, Japan Conference Date: 20010604-20010607
E.I. Conference No.: 58615
Source: IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD) 2001. p 445-448 (IEEE cat n 01CH37216)
Publication Year: 2001
CODEN: PISDEK
Language: English
Abstract: This report premieres to reveal remarkable characteristics of the newly invented 600V **CSTBT** (**Carrier Stored Trench-Gate Bipolar Transistor**). The essential significance of the characteristics is that the fabricated 600V/50A (equipped with an optimized CS-N layer) can achieve the level that on-state voltage is 1.22V (J//c=210A/cm**2) at Tj=25 degree C or 1.15V at Tj=125 degree C. Besides, benefited from its advanced structure, the 600V **CSTBT** possesses a more efficient trade-off characteristic between on-state voltage and turn-off loss than the conventional **TIGBT** does. In addition, the 600V **CSTBT** can be able to achieve the ideal turn-off capability, 2100A/cm**2 or over, by being reinforced by a finer emitter pattern and high-energy boron implant of P base layer. 5 Refs.

12/3,AB/8 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05482923
E.I. No: EIP00025041424
Title: New 1200V power modules with sophisticated **trench** gate **IGBT** and superior soft recovery diode
Author: Iwamoto, H.; **Takahashi, H.**; Tabata, M.; Satoh, K.
Corporate Source: Mitsubishi Electric Co, Fukuoka, Jpn
Conference Title: Proceedings of the 1999 3rd IEEE International Conference on Power Electronics and Drive Systems (PEDS'99)
Conference Location: Kowloon, Hong Kong Conference Date: 19990727-19990729
E.I. Conference No.: 55956
Source: Proceedings of the International Conference on Power Electronics and Drive Systems v 1 1999. p 28-33
Publication Year: 1999
CODEN: 85RTA3
Language: English
Abstract: A new PT-type **Trench** Gate **IGBT** has been developed using a local lifetime control in the n plus buffer layer. A prototype was developed after analyzing the device and estimating its characteristics using simulation. Both the result of simulation and that of measurement of the prototype have matched. Though the chip area is about 40-50% smaller than the conventional **IGBT**, the newly developed **IGBT**'s on-state voltage is about two-thirds (1.8V, typ.), its switching loss is about 80%, and has a larger reverse bias switching withstand capability. Also, a high-speed diode with excellent soft recovery characteristic was developed using local lifetime control in anode-side n-layer. As a result, a reduction of surge voltage, noise, and switching power loss has been achieved. This paper will present the structures and characteristics of the new **IGBT** and diode and their analysis result. (Author abstract) 7 Refs.

12/3,AB/9 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05192088
E.I. No: EIP98124510755
Title: Characteristics of a 1200 V PT **IGBT** with **trench** gate and local life time control
Author: Motto, Eric R.; Donlon, John F.; **Takahashi, H.**; Tabata, M.; Iwamoto, H.
Corporate Source: Powerex Inc, Youngwood, PA, USA
Conference Title: Proceedings of the 1998 IEEE Industry Applications Conference. Part 2 (of 3)
Conference Location: St.Louis, MO, USA Conference Date: 19981012-19981015
E.I. Conference No.: 49387
Source: Conference Record - IAS Annual Meeting (IEEE Industry Applications Society) v 2 1998. IEEE, Piscataway, NJ, USA,98CH36242. p 811-816
Publication Year: 1998
CODEN: CIASDZ ISSN: 0197-2618
Language: English
Abstract: A new 1200 V **IGBT** with a V//C//E(sat) of 1.9 V at 125 C and 140 A/cm**2 has been developed using a **trench** gate PT (punch-through) structure and local life time control. Compared to state-of-the-art third generation planar devices, this device represents a 30% improvement of on-state losses at almost twice the current density. This paper will describe the structure and characteristics of this new **IGBT**. (Author abstract) 11 Refs.

12/3,AB/10 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04815004
E.I. No: EIP97093816277
Title: Logic drive consideration for **trench**-gate **IGBT**
Author: **Takahashi**, **H.**; Takeda, M.; Hagino, H.; Yamada, T.
Corporate Source: Mitsubishi Electric Corp, Fukuoka-City, Jpn
Conference Title: Proceedings of the 1997 9th International Symposium on Power Semiconductor Devices and ICs, ISPSD
Conference Location: Weimer, Ger Conference Date: 19970526-19970529
E.I. Conference No.: 46957
Source: IEEE International Symposium on Power Semiconductor Devices & ICs (ISPSD) 1997. IEEE, Piscataway, NJ, USA,97CH36086. p 205-208
Publication Year: 1997
CODEN: PISDEK
Language: English
Abstract: This paper presents the initial consideration and the experimental results of logic gate drive used for **Trench**-gated **IGBT**(**TIGBT**). The Logic drive **IGBT** was examined by using a 600 V/50 A(j//c equals 200 A/cm**2) **TIGBT** with thin gate oxide and low threshold voltage and the **TIGBT** was driven at logic voltage level of V//G//E equals plus or minus 5 V. A V//C//E(sat) of 1.53 V with a turn off loss of 2 mJ/pulse was achieved. Furthermore, the turn-off capability of the **TIGBT** achieved almost full square characteristic. (Author abstract) 4 Refs.

12/3,AB/13 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

05007272 JICST ACCESSION NUMBER: 02A0022311 FILE SEGMENT: JICST-E
Wide cell pitch 1200V NPT CSTBTs with short circuit ruggedness.
NAKAMURA HIDEKI (1); NAKAMURA KATSUMI (1); KUSUNOKI SHIGERU (1);
TAKAHASHI HIDEKI (1); HARADA MASANA (1); TOMOMATSU YOSHIFUMI (2)
(1) Mitsubishi Electr. Corp.; (2) Fukuryosemikon'enjiniaringu
Denki Gakkai Denshi Debaisu Kenkyukai Shiryo, 2001, VOL.EDD-01,NO.76-88, PAGE.45-48, FIG.8, REF.3
JOURNAL NUMBER: Z0910AAZ
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: We have studied a suitable structure for 1200V NPT-IGBTs from the viewpoint of total performance. We propose the wide cell pitch **CSTBT** (**Carrier Stored Trench** Bipolar Transistor) structure. As a result, small gate capacitance and short circuit ruggedness have been established by reducing MOS channel width. And small on-state voltage has been achieved by carrier store effect of CSTBTs. To keep the breakdown voltage and to suppress the oscillation during short circuit operation, damping **trench** capacitors have been also prepared. (author abst.)

12/3,AB/15 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02008201 JICST ACCESSION NUMBER: 94A0361355 FILE SEGMENT: JICST-E
A 600V Gate-Insulated Bipolar Transistor Using a **Trench** MOS Gate.
HARADA MASANA (1); MINATO TADAHIRO (1); TAKADA IKUNORI (1); **TAKAHASHI HIDEKI** (2); INOUE KEIJI (2); NISHIHARA HIDENORI (3)
(1) Mitsubishidenki ULSIKaiken; (2) Mitsubishi Electric Corp., Fukuoka Machinery Works; (3) Mitsubishi Electric Corp., Kitaitami Machinery Works
Mitsubishi Denki Giho, 1994, VOL.68,NO.3, PAGE.270-274, FIG.11, REF.6
JOURNAL NUMBER: F0198AAP ISSN NO: 0369-2302 CODEN: MTDNA
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: The corporation has developed a 600V/50A insulated-**gate bipolar transistor** (**IGBT**) with a **trench** MOS-gate structure. As a result of this **trench** MOS-gate structure, the new **IGBT** has a cell area one-tenth that of previous IGBTs, sustains a maximum current density of 200A/cm2, turns on at the unusually low level of 1.4V (tf=200ns), and has a high breakdown voltage. Tests on these **trench** IGBTs showed their characteristics to be nearly ideal. (author abst.)

14/3,AB/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04464740
E.I. No: EIP96083273093
Title: 5- mu m**2 full-CMOS cell for high-speed SRAMs utilizing a optical-proximity-effect correction (OPC) technology
Author: Ueshima, Masahiro; Mano, Michio; Yoneda, Yutaka; Ichikawa, Tsutomu; Tsudaka, Keisuke; **Takahashi, Hiroshi**; Yamamura, Ikuhiro; Yabuta, Mitsuo; Motoyoshi, Makoto
Corporate Source: Sony Corp, Kanagawa, Jpn
Conference Title: Proceedings of the 1996 Symposium on VLSI Technology
Conference Location: Honolulu, HI, USA Conference Date: 19960611-19960613
E.I. Conference No.: 45102
Source: Digest of Technical Papers - Symposium on VLSI Technology 1996. IEEE, Piscataway, NJ, USA,96CH35944. p 146-147
Publication Year: 1996
CODEN: DTPTEW ISSN: 0743-1562
Language: English
Abstract: A 5.01- mu m**2 full-CMOS SRAM cell using a 0.28- mu m design rule has been developed and the cell operation at as low as 0.6V was confirmed. This cell has been designed not only to be small but also to be widened bitline pitch for reduction of bitline delay. To realize this cell, optical-proximity-effect correction (OPC) and some technologies for cell-size reduction have been adopted. In addition, glue layer wiring (GLAW) for the local interconnection has been used in order to simplify the process. (Author abstract)

14/3,AB/2 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02636581 JICST ACCESSION NUMBER: 95A0734188 FILE SEGMENT: JICST-E
Synchronous Rectifiers Using The **Trenched** Gate Power MOSFET.
FUKUMOCHI YASUAKI (1); **TAKAHASHI HIDEKI** (1); ONO TAKASHI (1); SUGA IKURO (2)
(1) Mitsubishi Electr. Corp.; (2) Mitsubishi Electr. Corp., Ind. Electron. & System. Dev. Lab.
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1995, VOL.95,NO.192(PE95 7-12), PAGE.29-35, FIG.7, TBL.5, REF.2
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.311.6 621.382.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: In order to reduce ON resistance and drive power of power MOSFET, we have developed 4V drive's and 2.5V drive's for the power MOSFET with **trench** gate structure. This paper describes the technology involved in developing this structure and its features. Also, experimental varification of the **trenched** gate power MOSFET is done using it on the 2'ry side of an actual DC-DC converter application. As a result, it is found that low voltage drive power MOSFET shows excellent performance is such application and proves to be a sure choice for elevating the overall efficiency of power conversion systems. (author abst.)

17/3,AB/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01892619 JICST ACCESSION NUMBER: 93A0841260 FILE SEGMENT: JICST-E
Application of AlGaAs/GaAs HBT's to Power Devices for Digital Mobile Radio Communications.
GOTO N (1); HAYAMA N (1); **TAKAHASHI H** (1); HONJO K (1)
(1) NEC Corp., Tsukuba-shi, JPN
IEICE Trans Electron(Inst Electron Inf Commun Eng), 1993, VOL.E76-C,NO.9, PAGE.1367-1372, FIG.10, TBL.2, REF.9
JOURNAL NUMBER: L1370AAA ISSN NO: 0916-8524
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3 621.396.73
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: This paper describes the performance of Al GaAs/GaAs HBT's developed for power applications. Their applicability to power amplifiers used in digital mobile radio communications is examined through measurement and numerical simulation, considering both power capability and linearity. Power HBT's with carbon-**doped** base layers showed DC current gains over 90. A linear gain of 19.2dB, a maximum output RF power of 32.5dBm, and a power added efficiency of 56 percent were obtained at 950MHz. Numerical simulations showed that the power efficiency of HBT amplifiers could be improved by using harmonic trap circuits. Intermodulation measurements showed that third-order distortions were at most -21dBc level at the 1-dB gain compression point. RF spectrum simulations using .PI./4 shift QPSK modulation showed that side-band spectrum generation was less than -45dBc level at points 50kHz off of the carrier frequency. These properties indicate that the power handling capabilities and linearity of HBT amplifiers offer promising potentials for digital mobile radio communications. (author abst.)

09/04/2002 09/896,161

19/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

03421874 INSPEC Abstract Number: A89094565
Title: Electrical and optical properties of poly(3,4-dialkythiophene)
Author(s): Yoshino, K.; Manda, Y.; Sawada, K.; Morita, S.; **Takahashi, H.**; Sugimoto, R.; Onoda, M.
Author Affiliation: Dept. of Electronic Eng., Fac. of Eng., Osaka Univ., Japan
Journal: Journal of the Physical Society of Japan vol.58, no.4 p. 1320-4
Publication Date: April 1989 Country of Publication: Japan
CODEN: JUPSAU ISSN: 0031-9015
Language: English
Abstract: Poly(3,4-dialkylthiophene) films prepared by both electrochemical and chemical methods utilizing FeCl/sub 3/ as a catalyst exhibit much larger band gap compared with non-substituted and 3-substituted polythiophene films. Poly(3,4-dialkylthiophene)s with long alkyl chains are soluble in several solvents. However, thermochromism has not been found contrary to poly(3-alkylthiophene), which is explained in terms of large torsion angle between neighbouring thiophene rings due to the steric hindrance by the bulky alkyl group. Poly(3,4-dimethylthiophene) with large band gap also demonstrates drastic spectral, electron spin resonance (ESR) and conductivity changes upon **doping** due to an insulator-metal transition.
Subfile: A

19/3,AB/2 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04252187 JICST ACCESSION NUMBER: 99A0662859 FILE SEGMENT: JICST-E
Removal of gaseous organic **impurities** using a ceramic chemical filter.
SAKATA SOICHIRO (1); **TAKAHASHI HIDETO** (1); SATO KATSUMI (1)
(1) Takasago Therm. Eng. Co., Ltd.
Kuki Seijo to Kontamineshyon Kontororu Kenkyu Taikai Yokoshu, 1999, VOL.17th, PAGE.48-50, FIG.3, TBL.2, REF.5
JOURNAL NUMBER: Y0789AAO
UNIVERSAL DECIMAL CLASSIFICATION: 628.84+697.94 614.71/.73:551.51 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Short Communication
MEDIA TYPE: Printed Publication
ABSTRACT: In the advanced **semiconductor** manufacturing process, the organic airbone-molecular-contaminants, AMCs, of a minute quantity which exist in clean rooms and adhere predominantly to wafer surfaces cause the **insulator** deterioration of oxide **films**, the inferior contact of resist films and the clouds of exposure lenses and mirrors. For the removal of organic AMCs in clean rooms, activated charcoal chemical filters have been installed in the air-flow paths. The conventional charcoal filters have a defect in release of adsorbed organic AMCs, dust generation for use in clean rooms, and a short life duration such as several months. We have newly developed a non-flammable ceramic chemical filter. It has a much higher removal efficiency of organic AMCs, a much longer life duration, and a much lower price than a conventional charcoal filter. (author abst.)

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